

Fig. 1 (PRIOR ART)

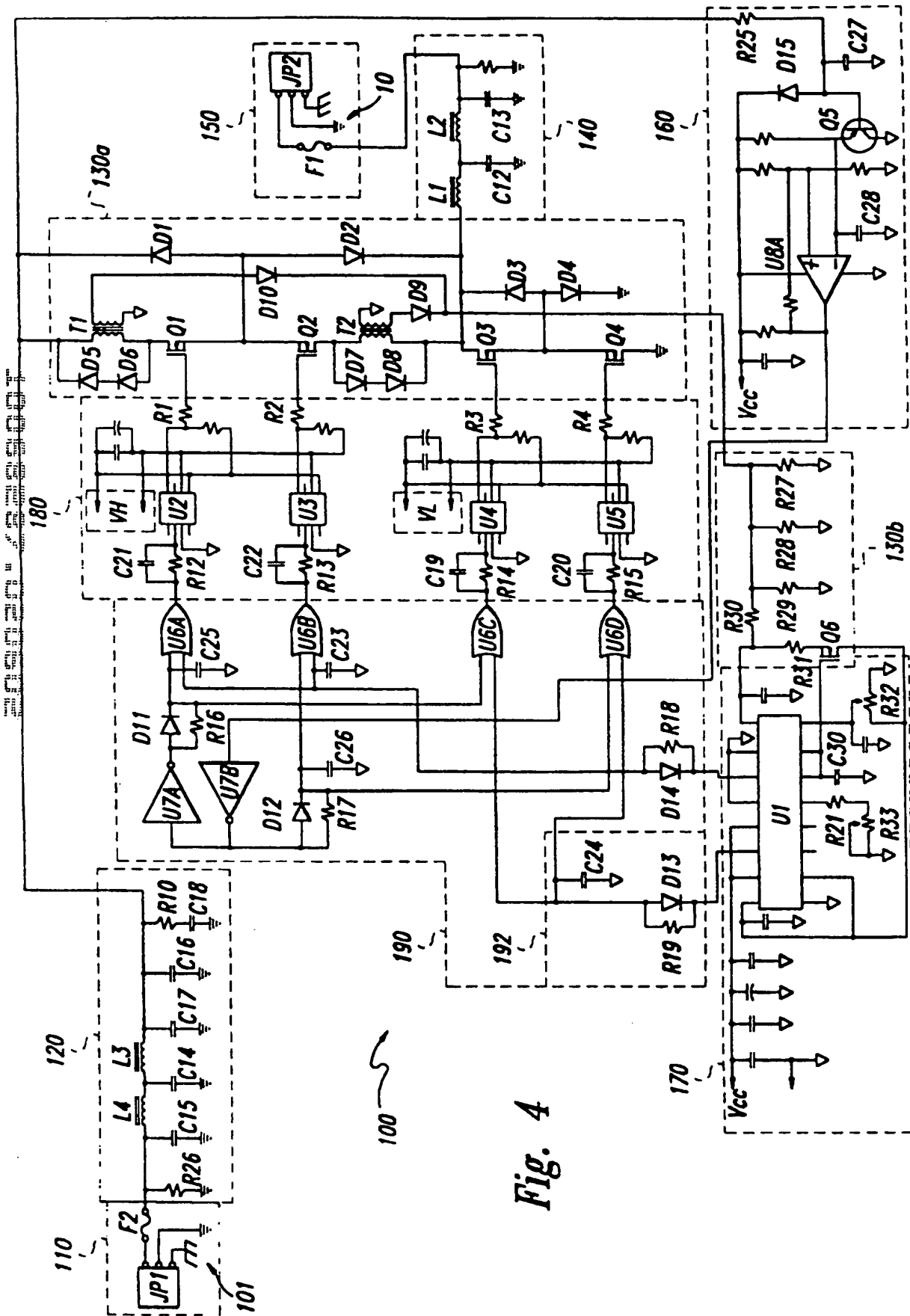


Fig. 4

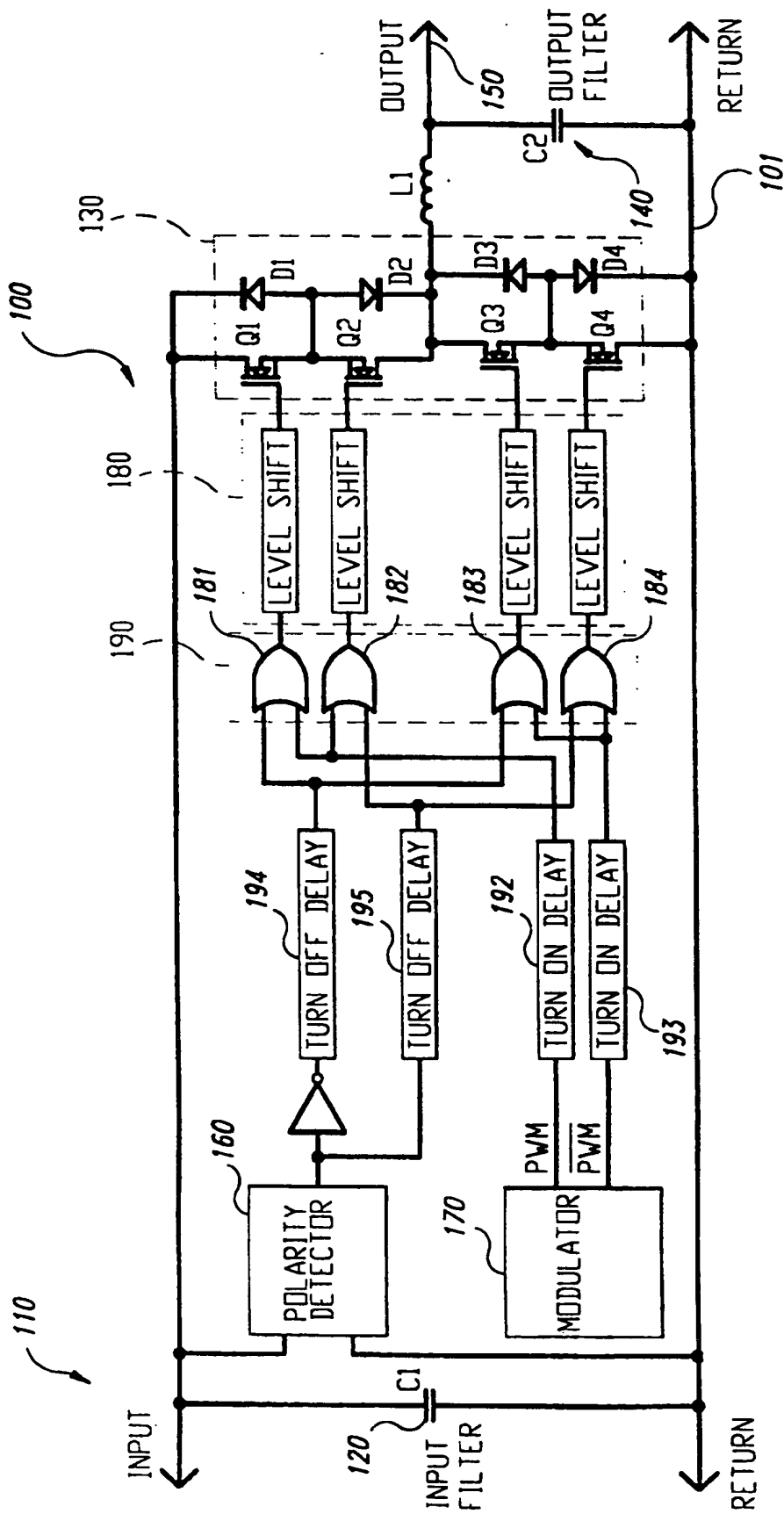


Fig. 5

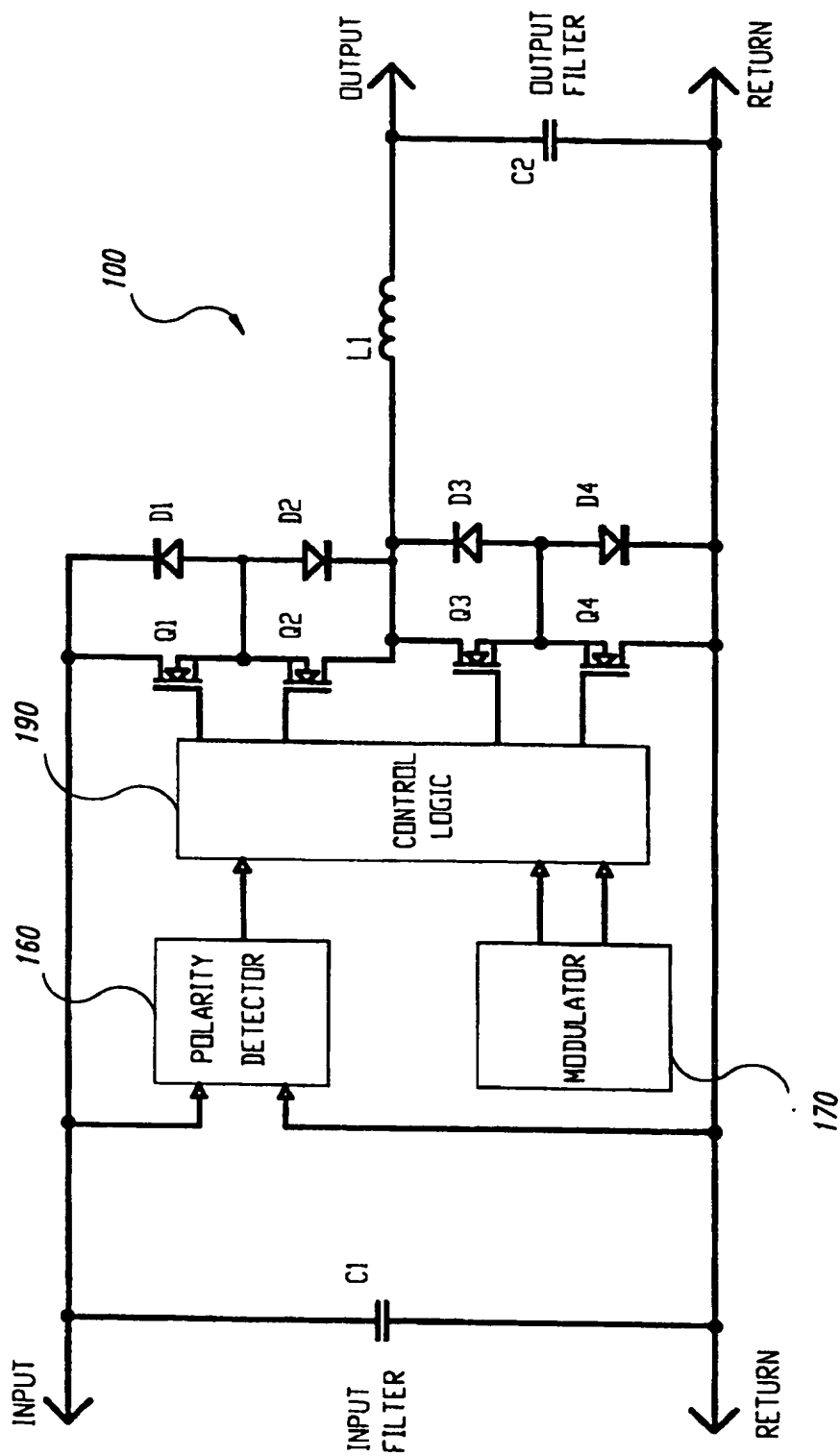


Fig. 6A

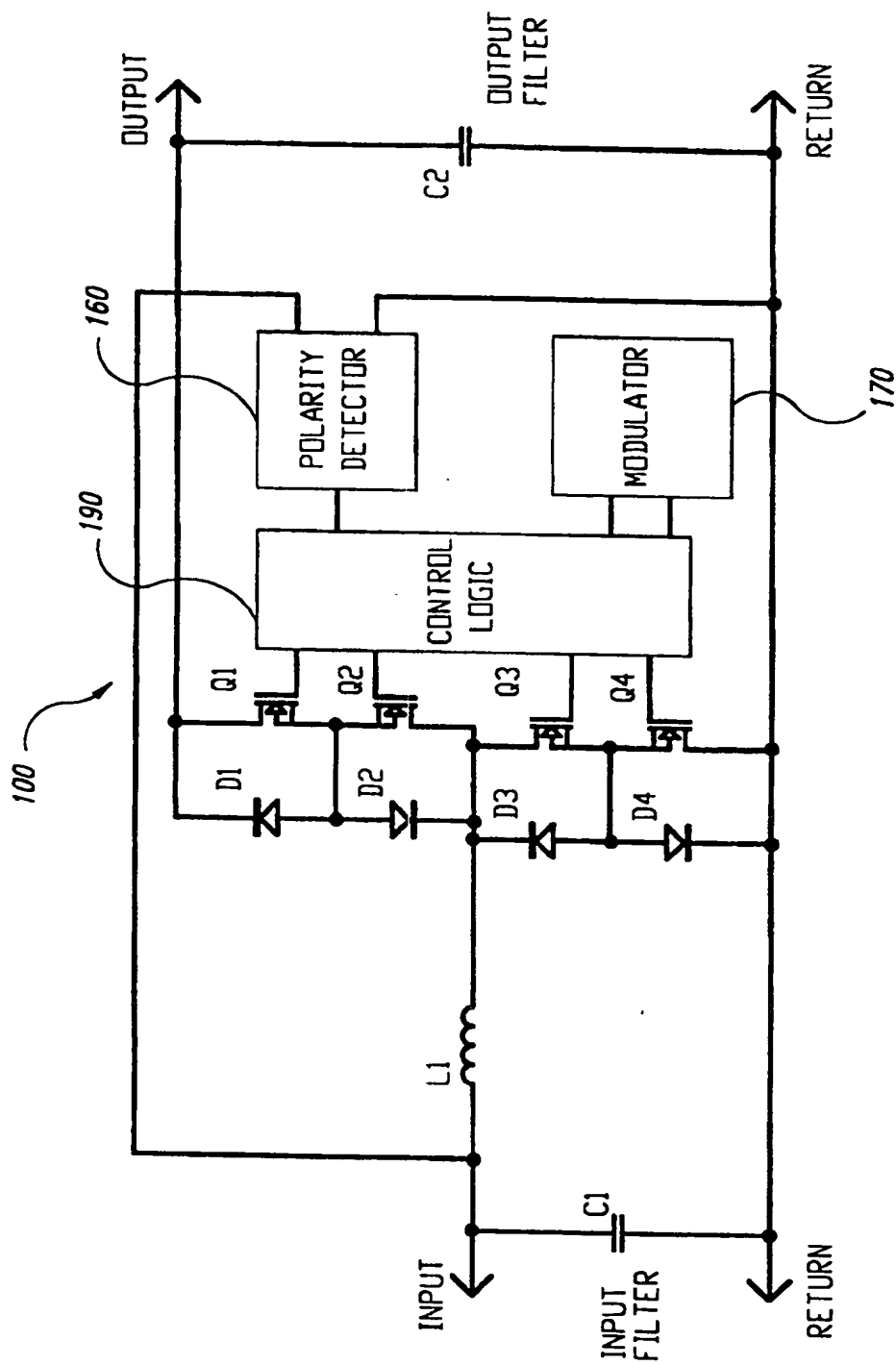


Fig. 6B

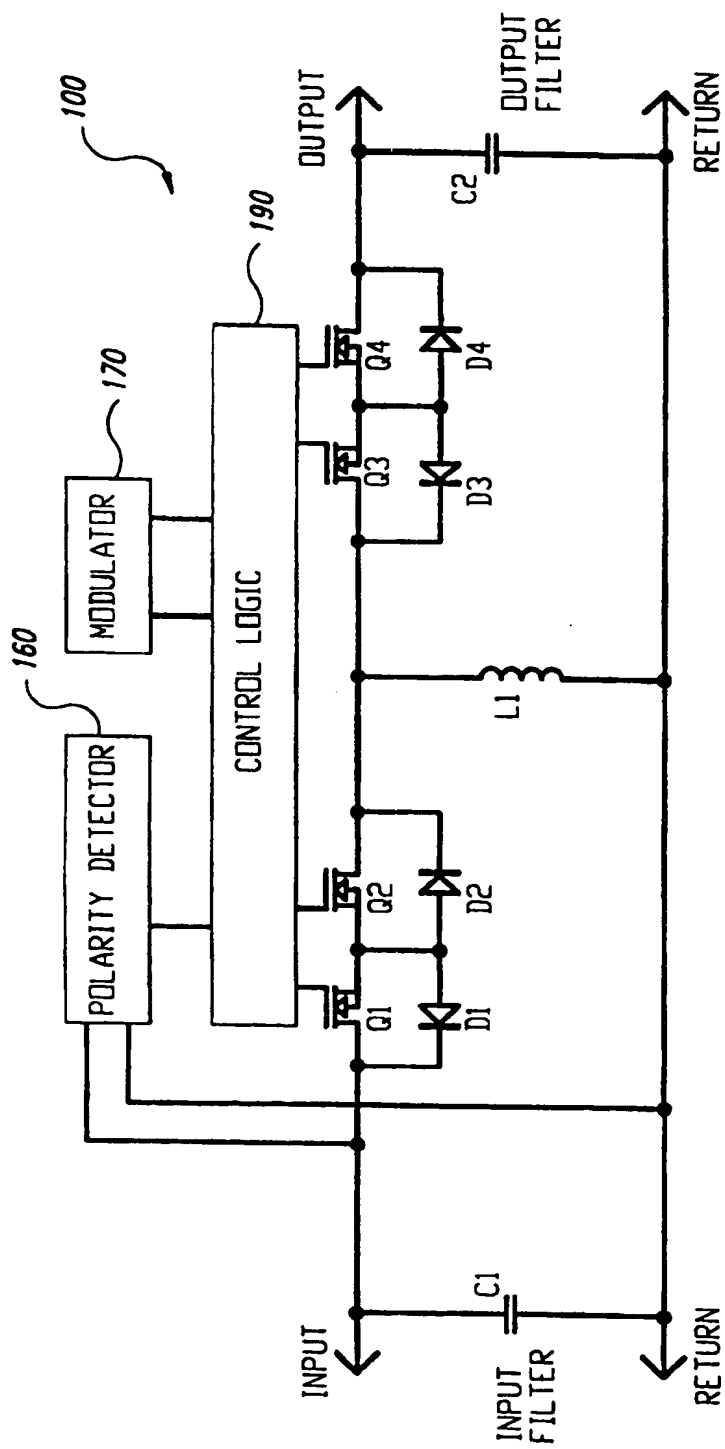


Fig. 6C

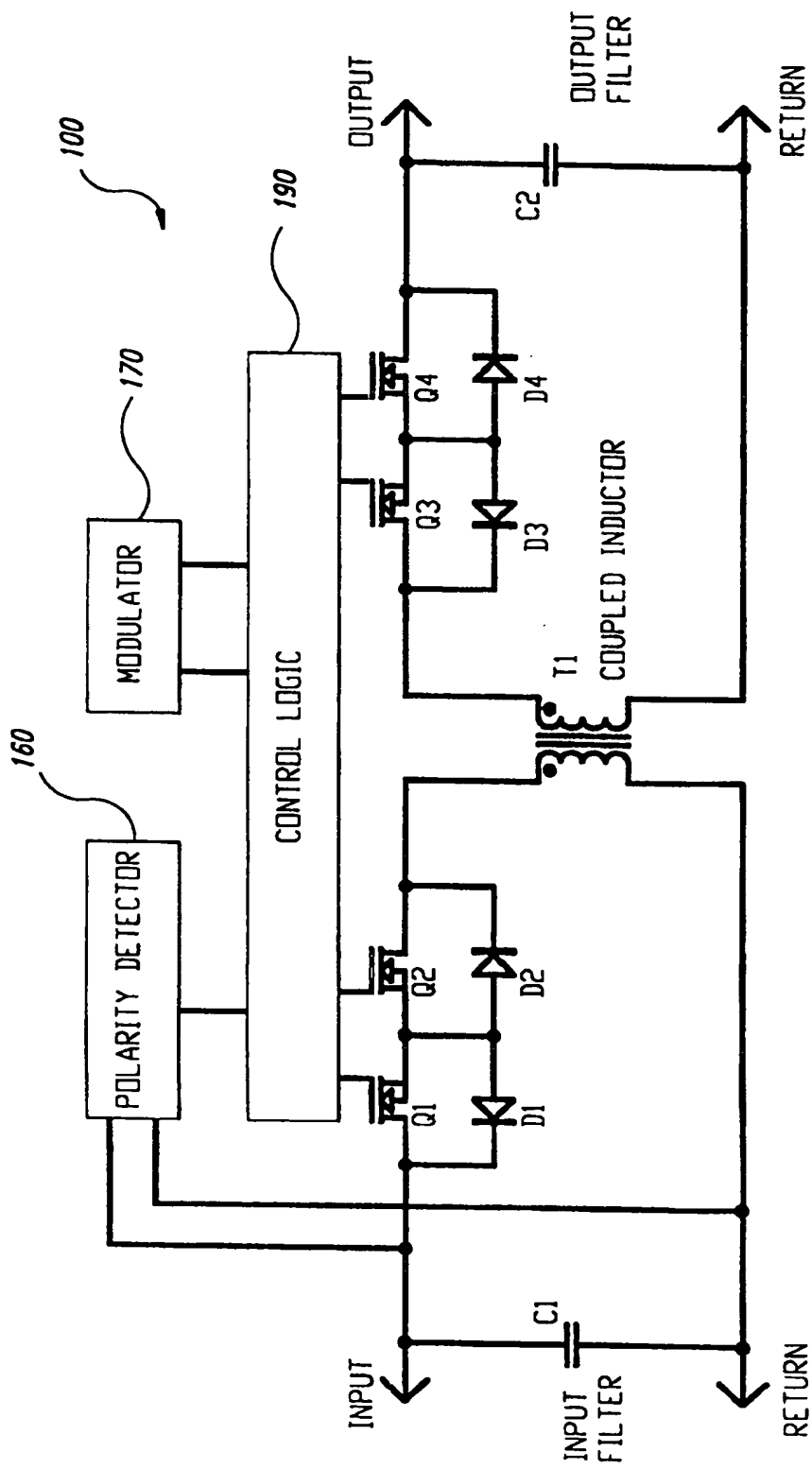


Fig. 6D

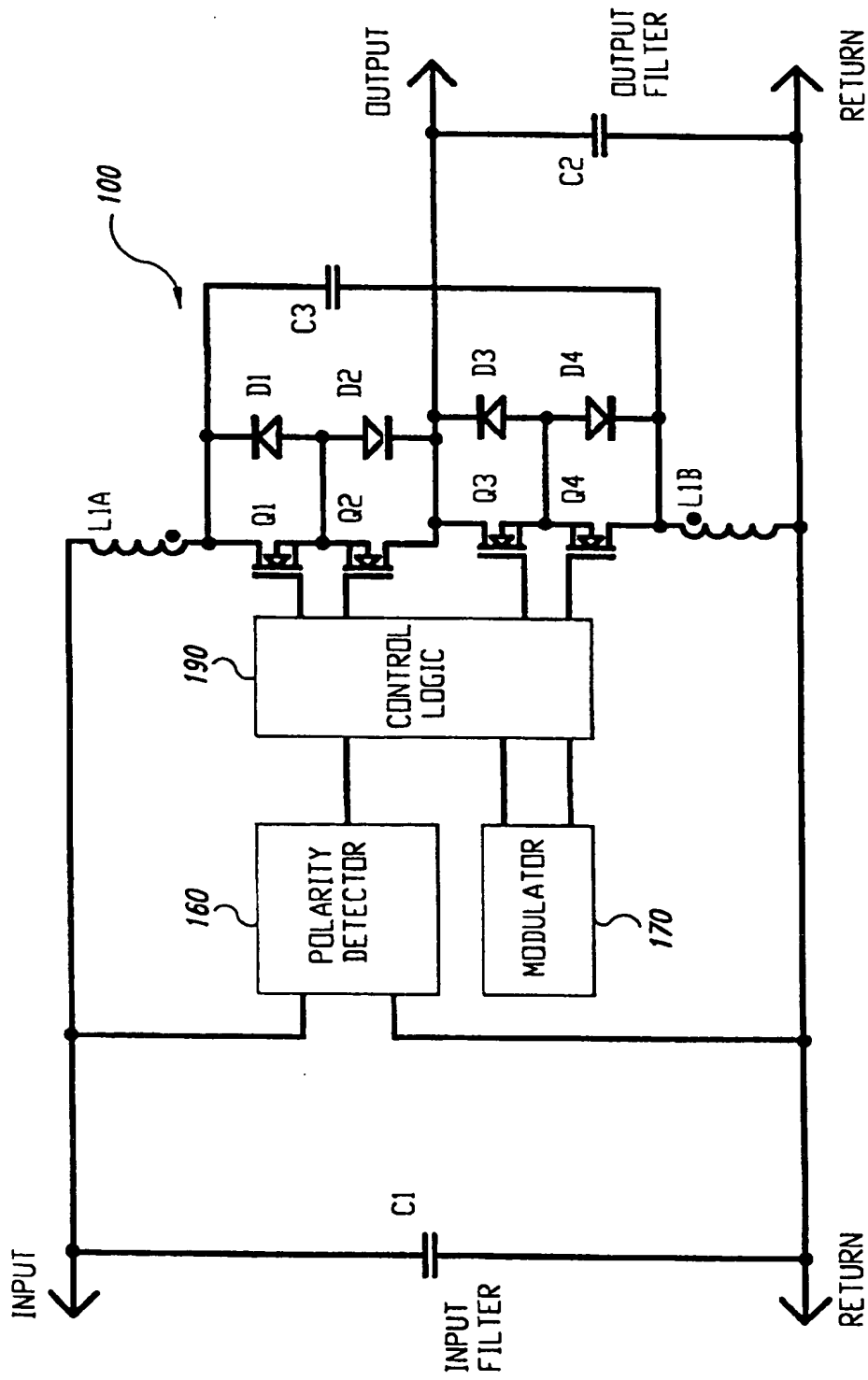


Fig. 7A

FIG. 7B is a schematic diagram of a power supply circuit 100. The circuit includes an input filter capacitor C1 connected between the input and return lines. The input is connected to a bridge rectifier consisting of four diodes D1, D2, D3, and D4. A capacitor C3 is connected across the bridge output. The bridge output is connected to a full-bridge inverter consisting of four MOSFETs Q1, Q2, Q3, and Q4. The gates of the MOSFETs are driven by a control logic block 190, which is connected to a polarity detector 160 and a modulator 170. The output of the inverter is connected to an output filter capacitor C2, which is connected to the output and return lines. The output is labeled 100.

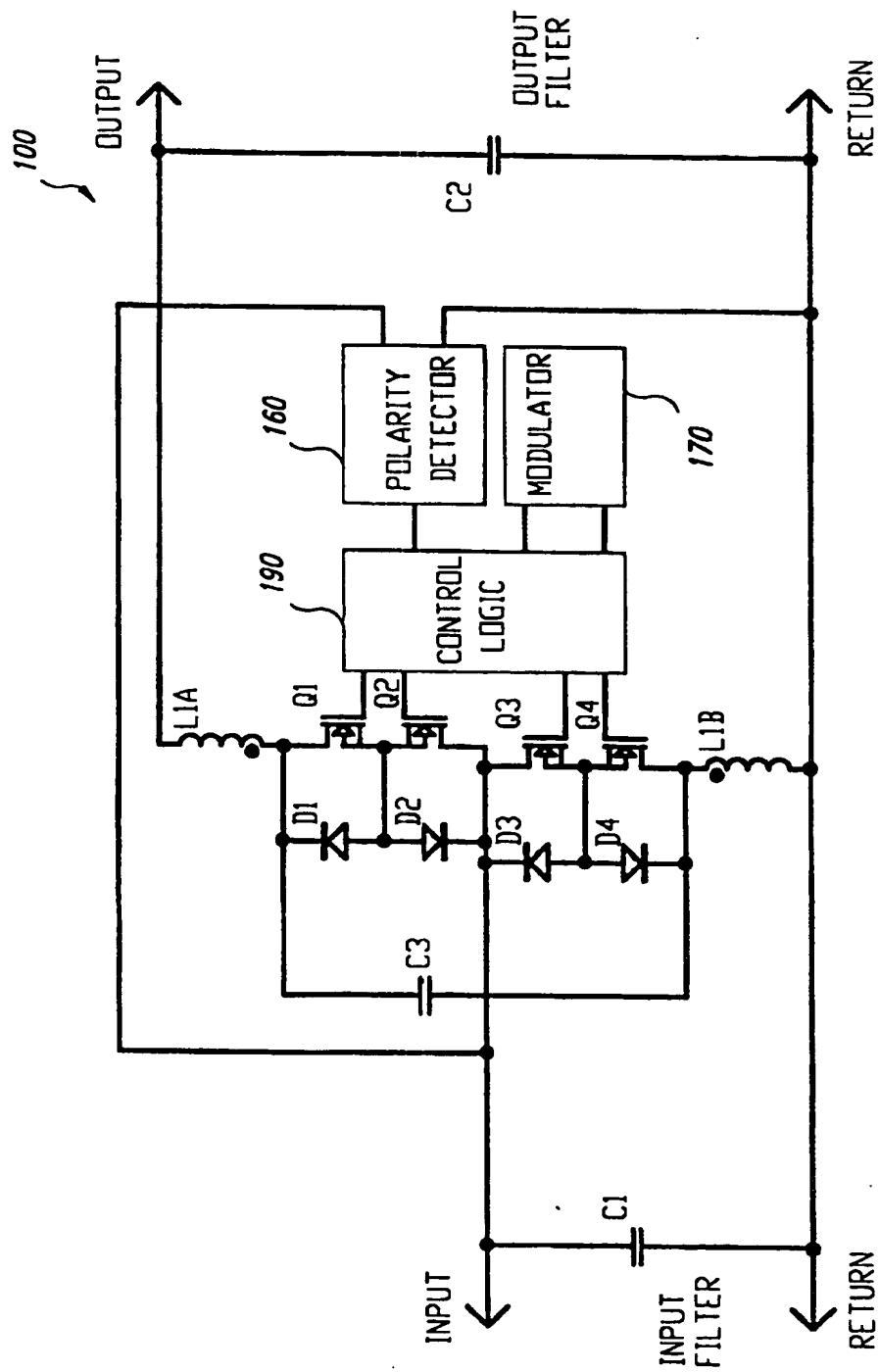


Fig. 7B

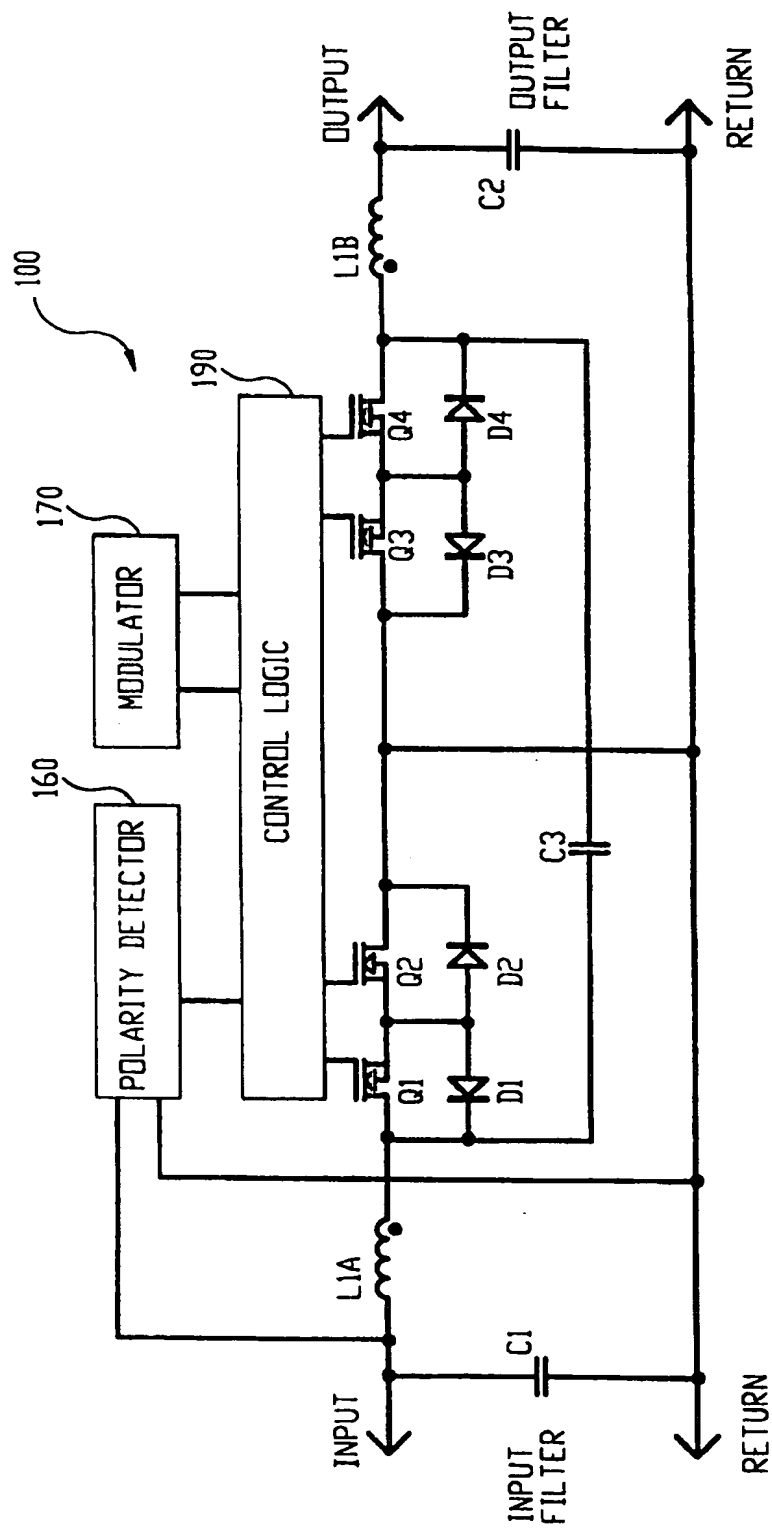


Fig. 7C

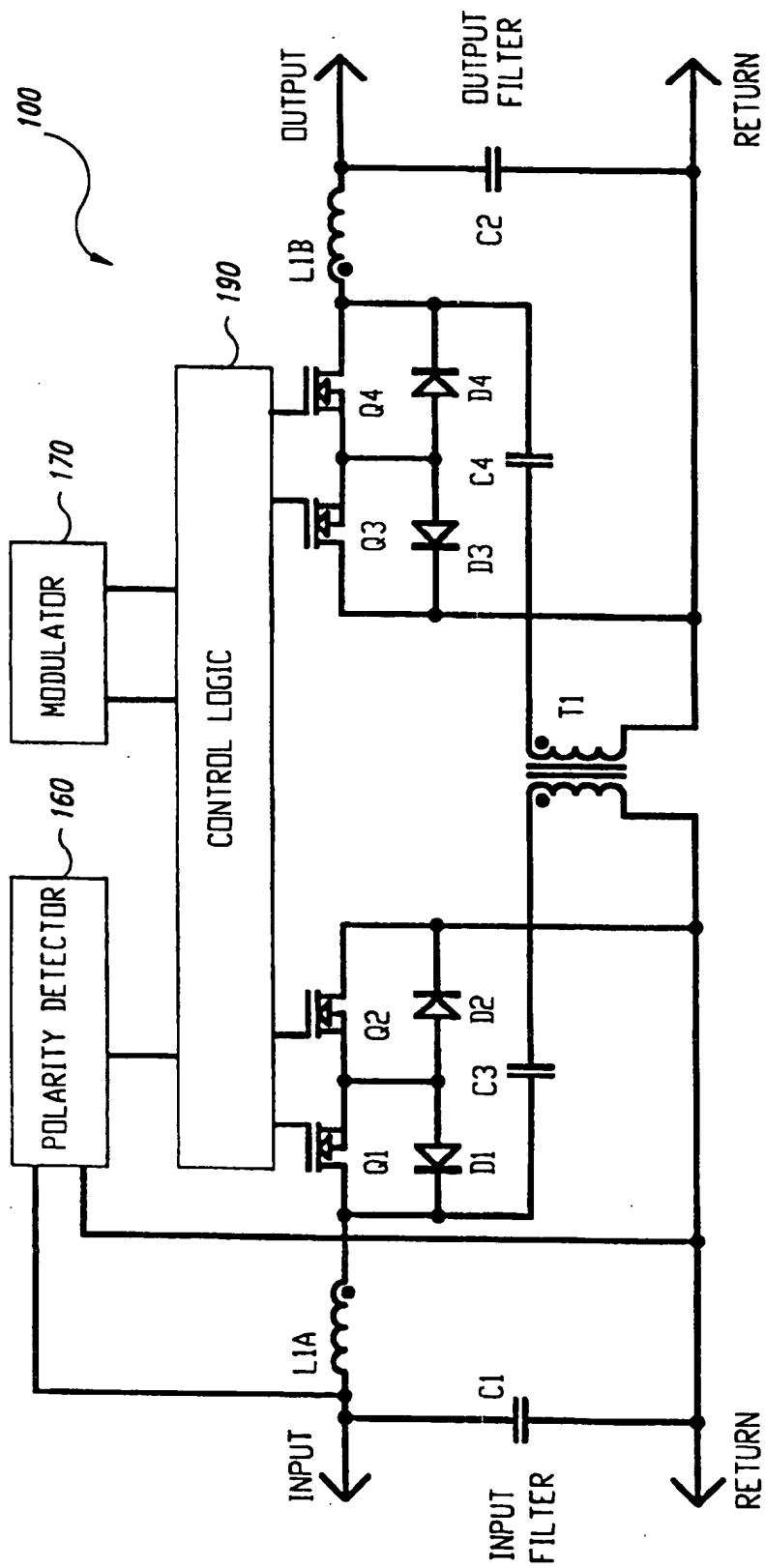


Fig. 7D

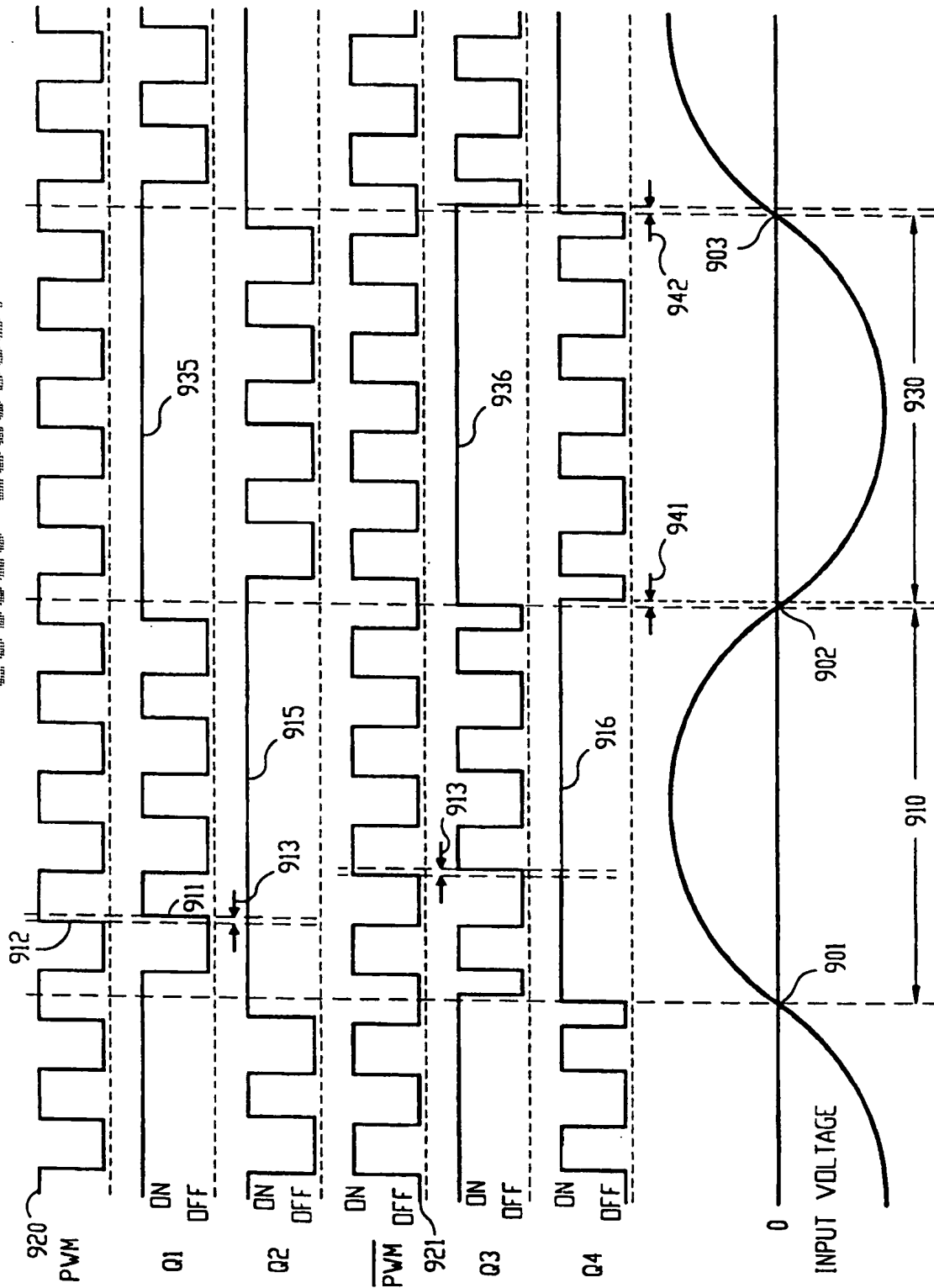


Fig. 8

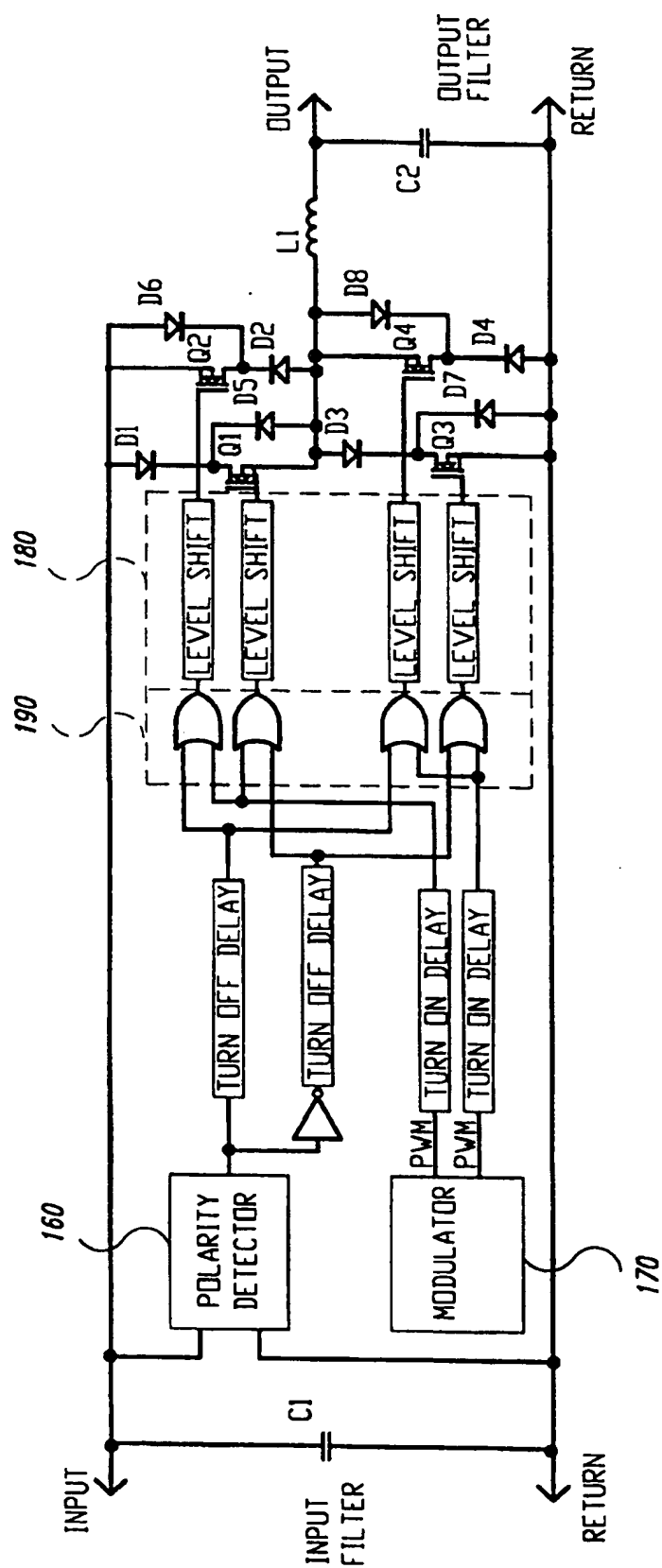


Fig. 9

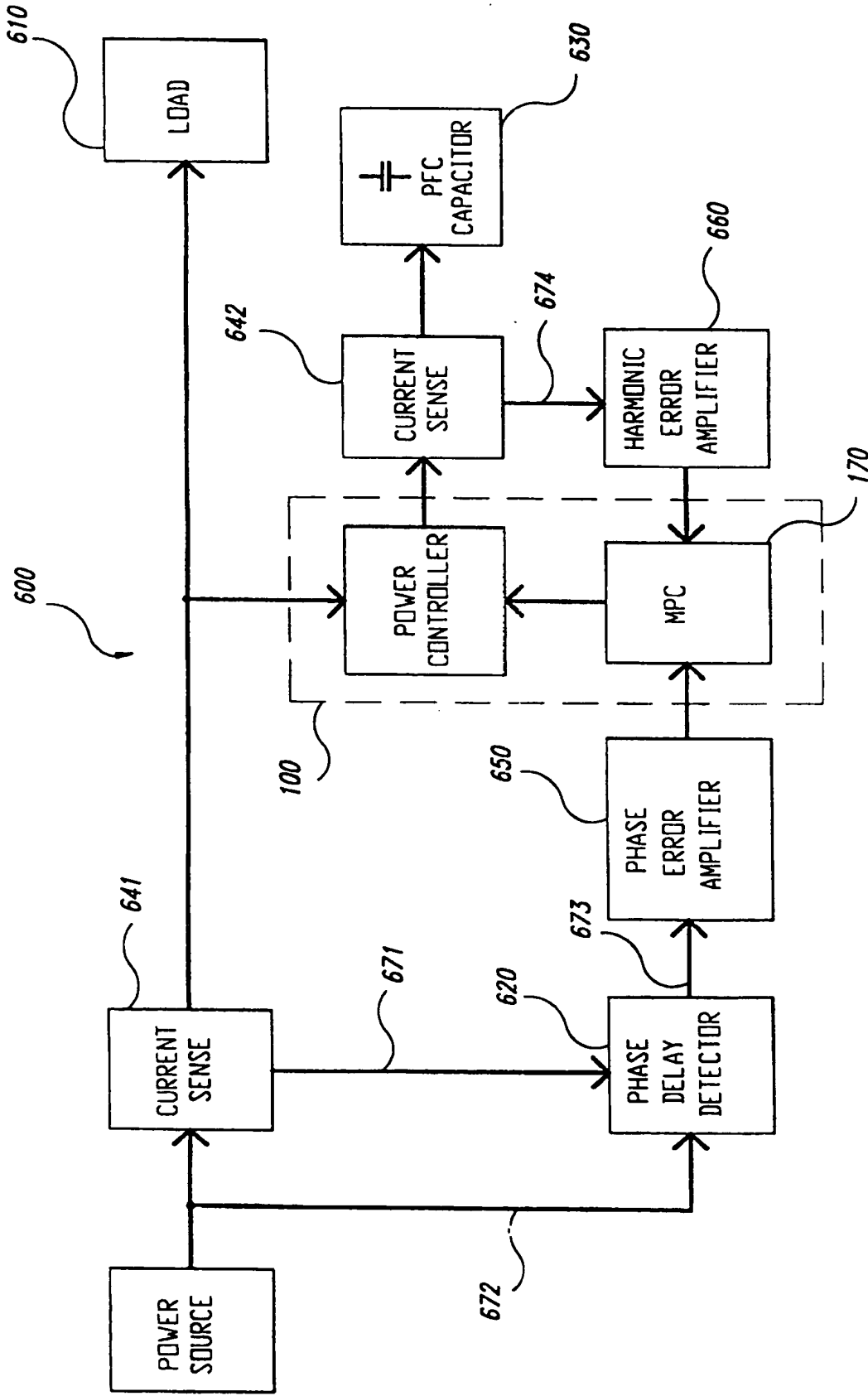


Fig. 10

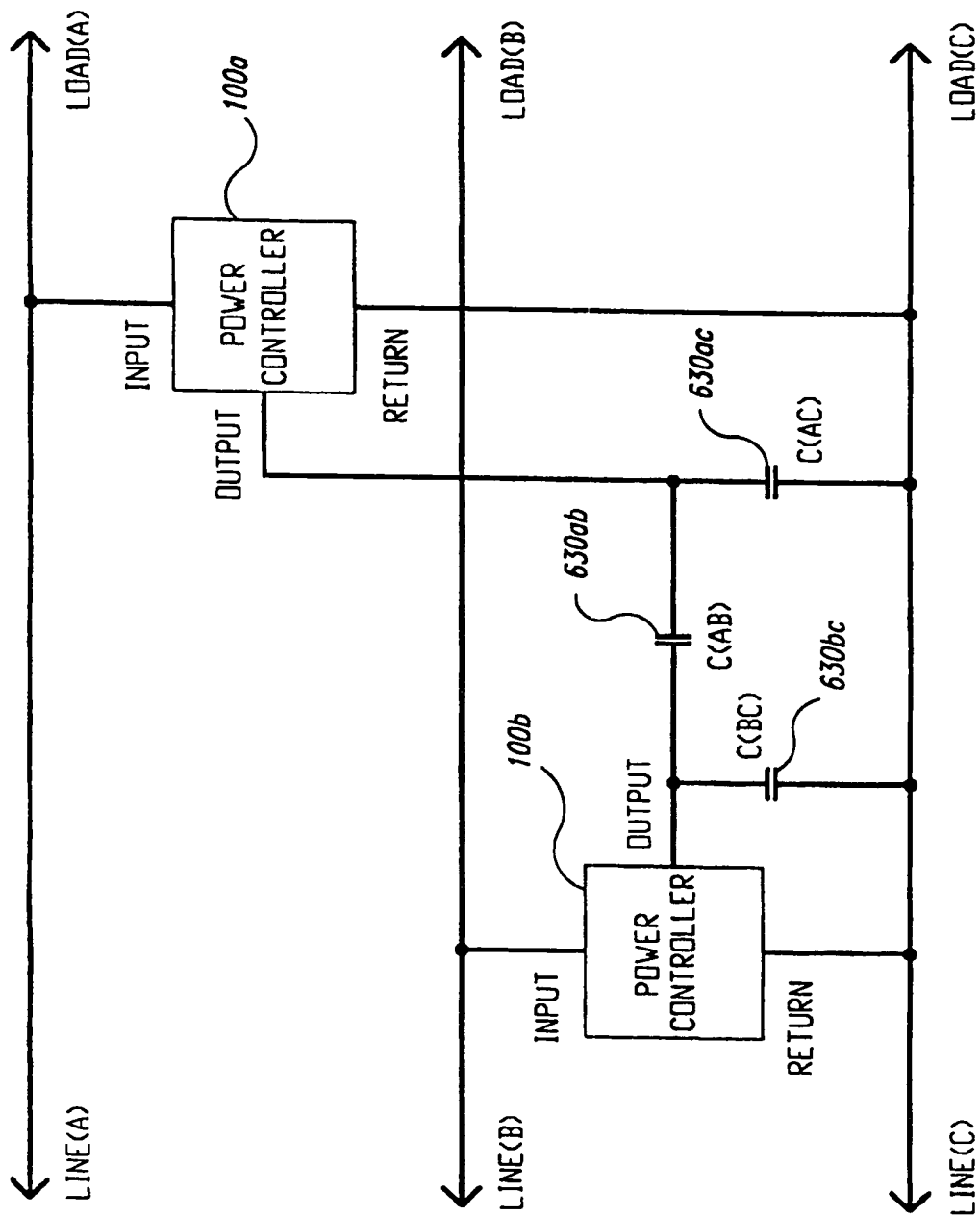


Fig. 11

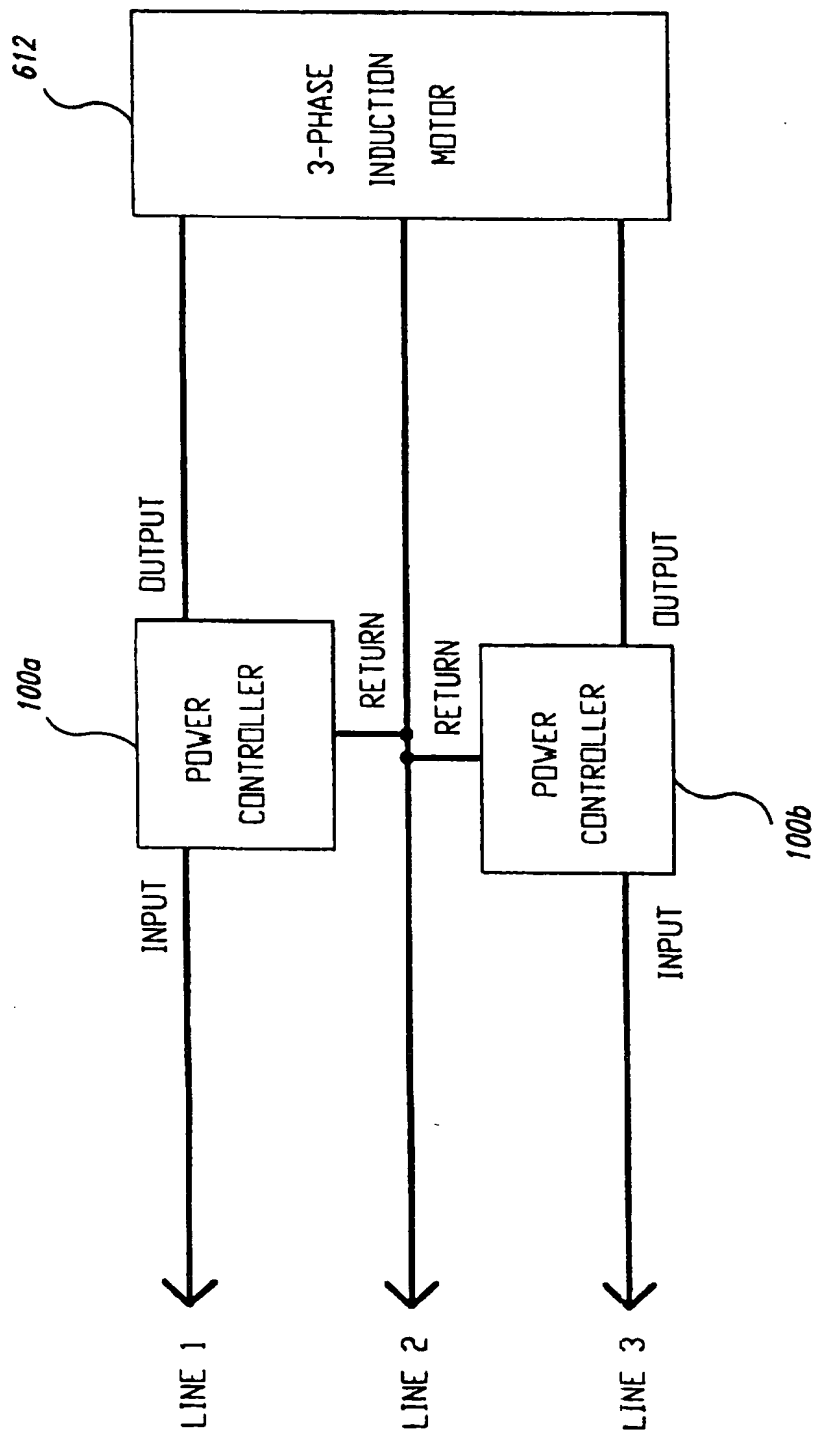


Fig. 12

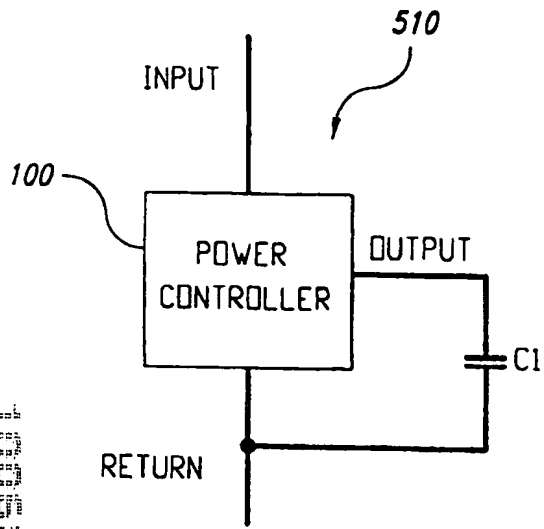


Fig. 13

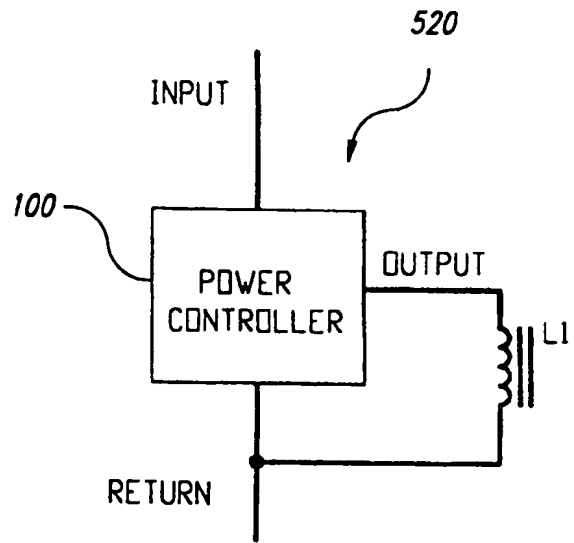


Fig. 14

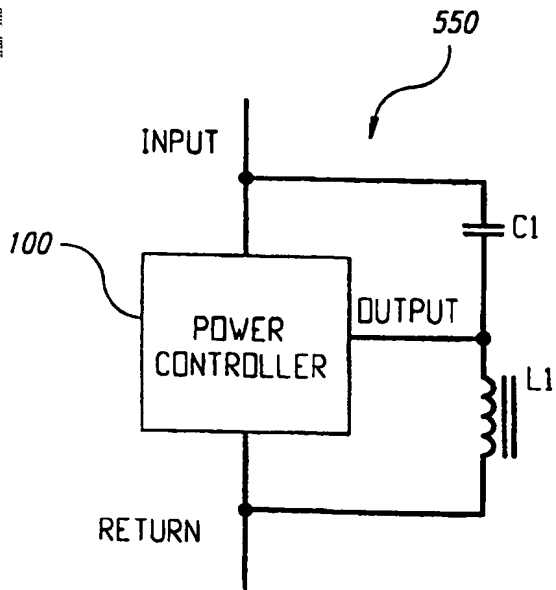


Fig. 15

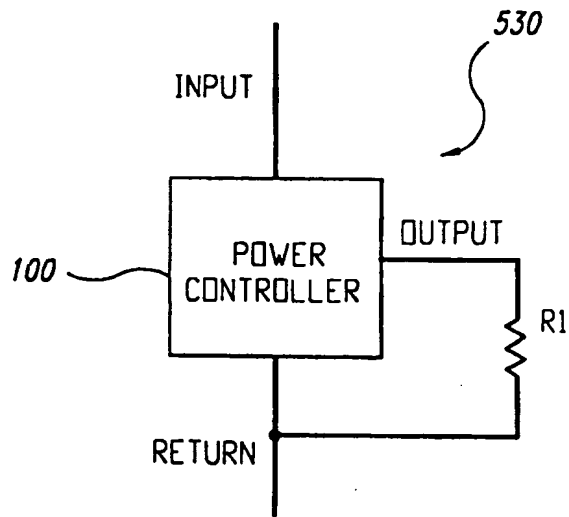


Fig. 16

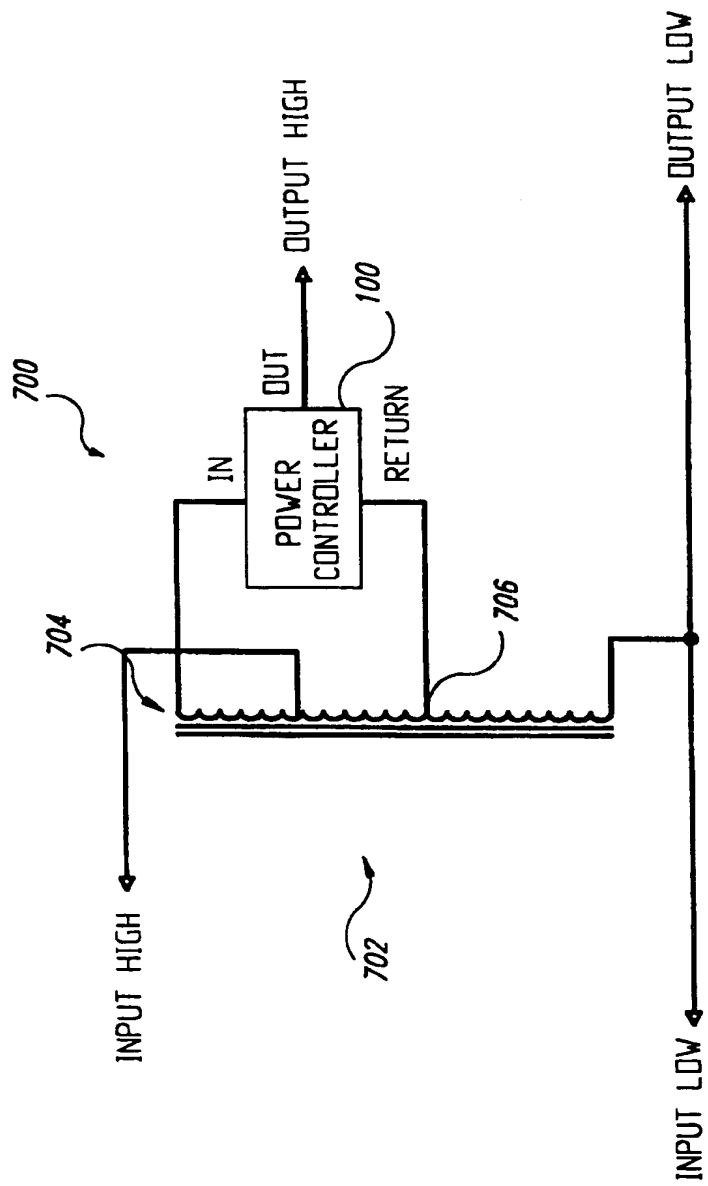


Fig. 17

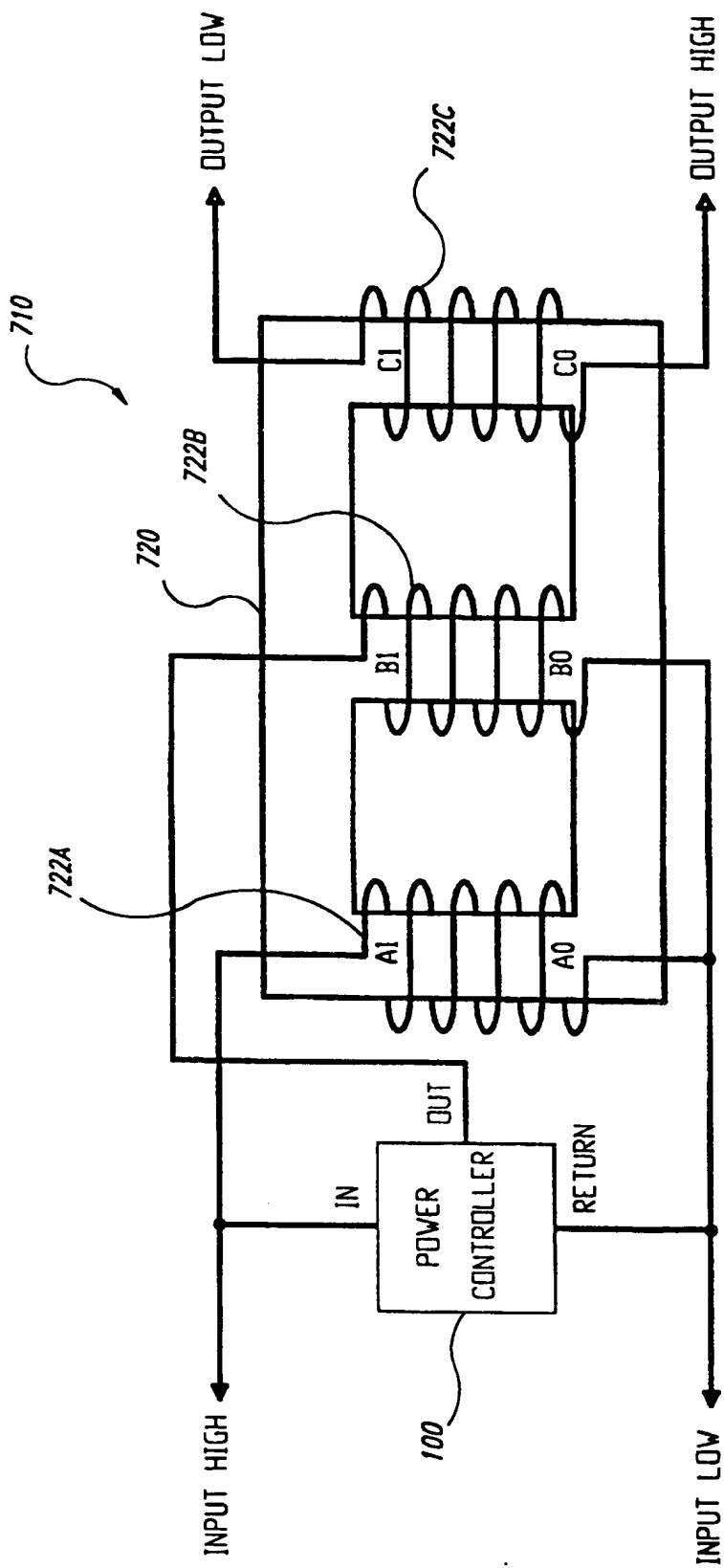


Fig. 18

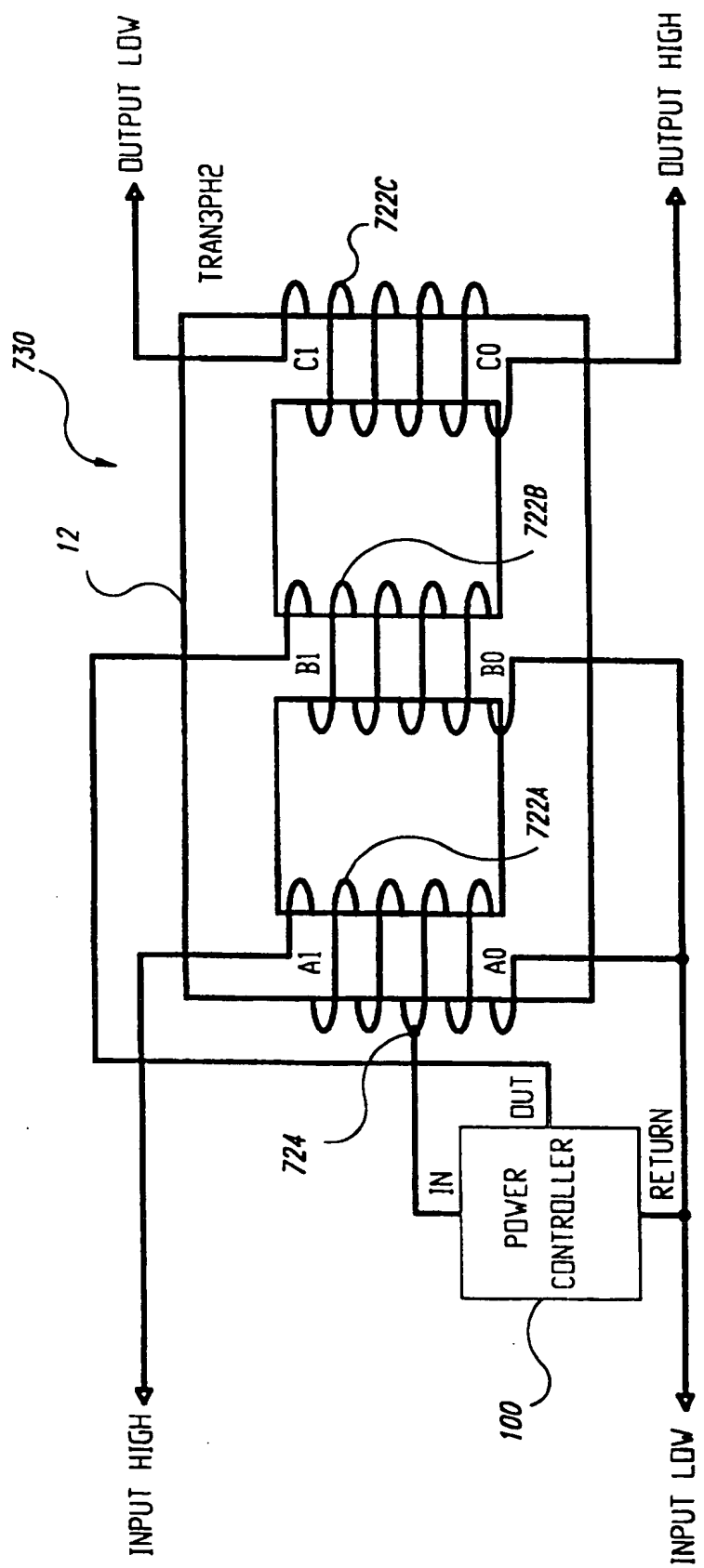


Fig. 19

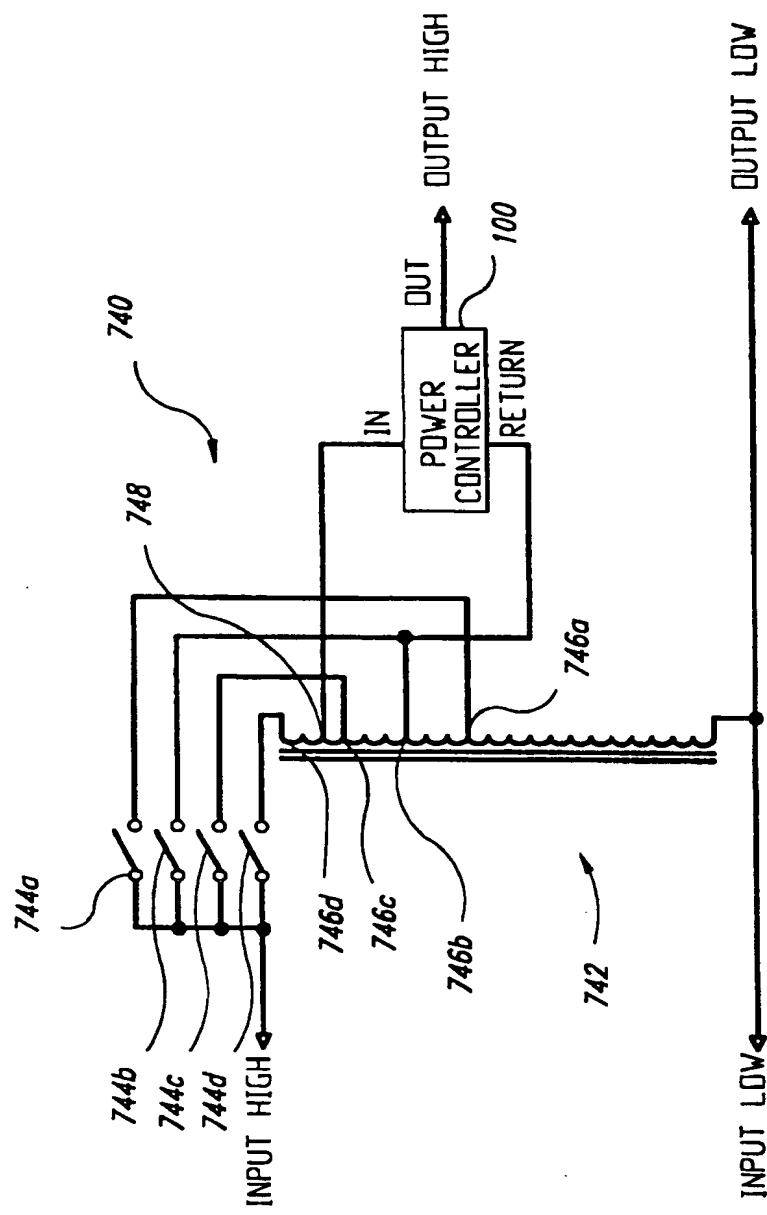


Fig. 20

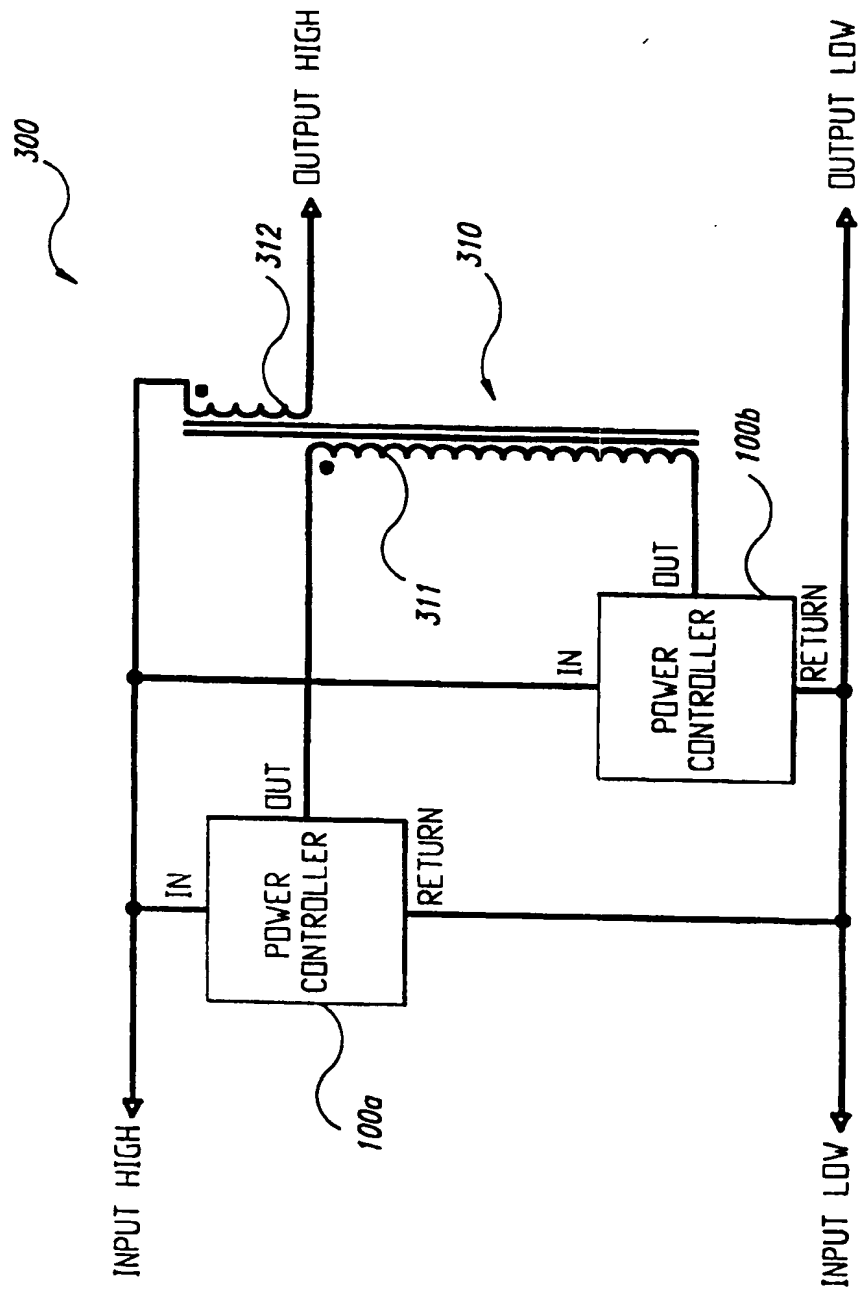


Fig. 22

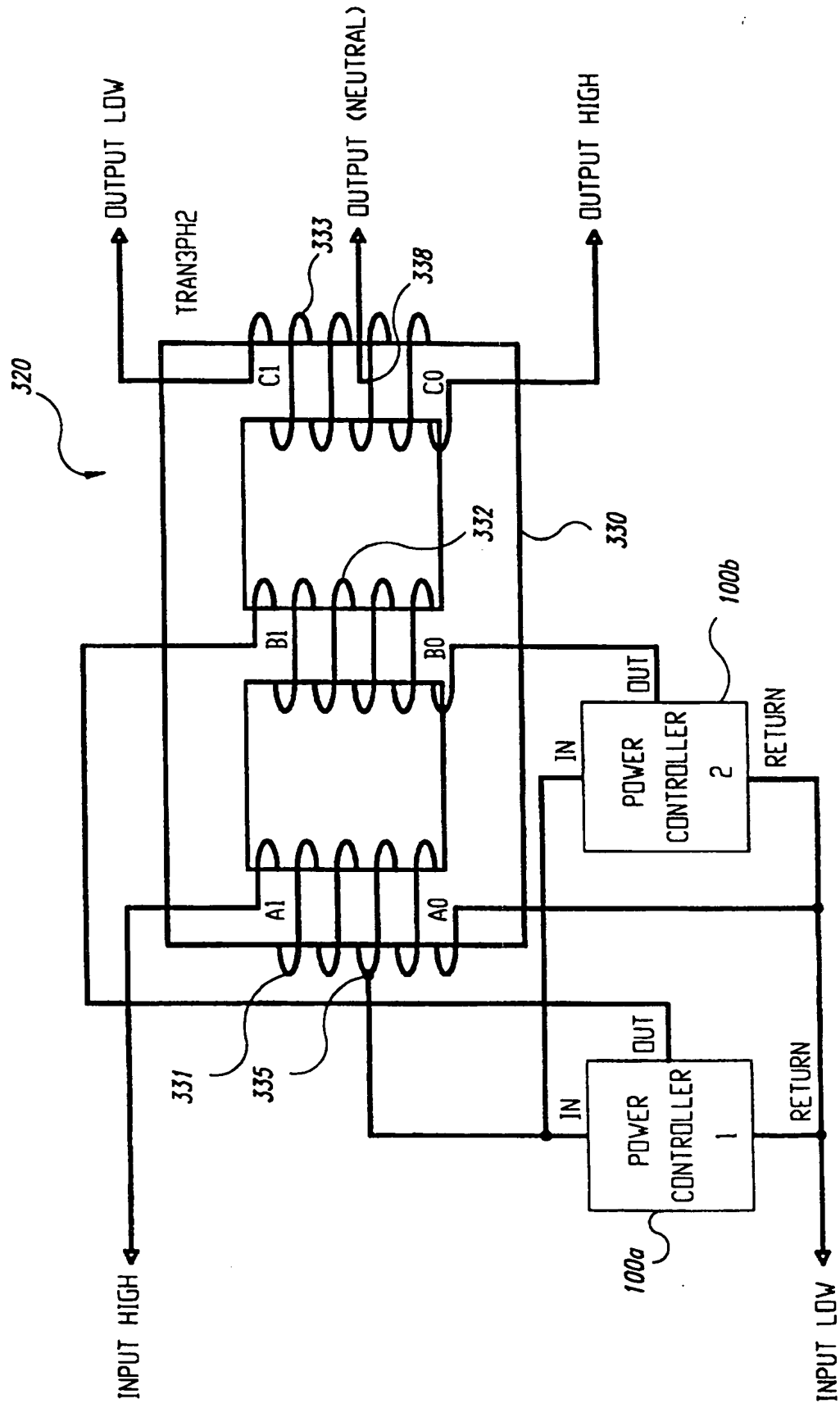


Fig. 23

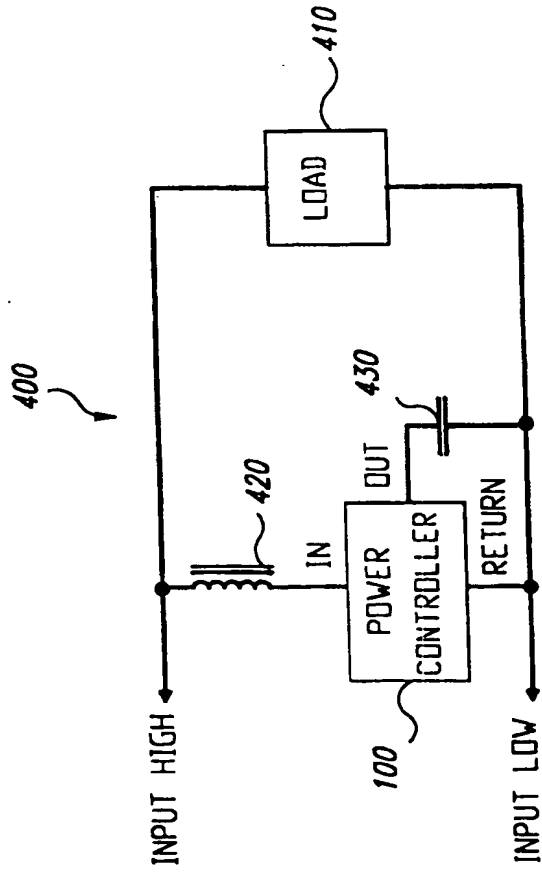


Fig. 24

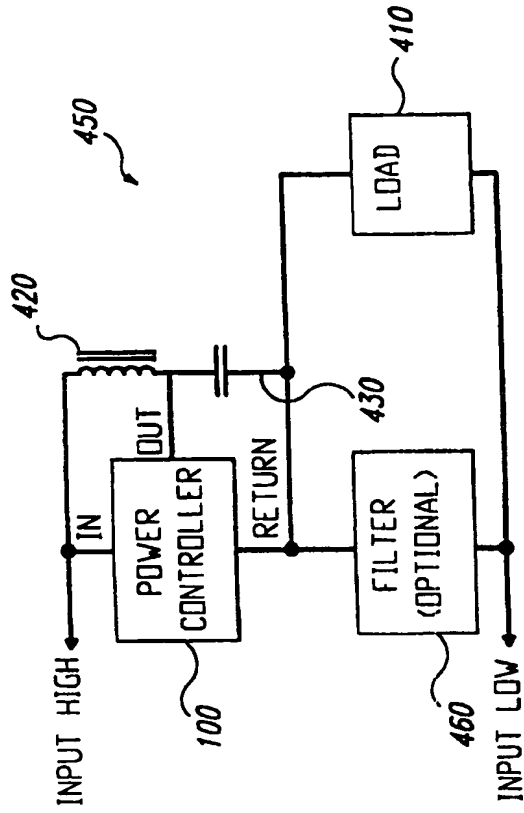


Fig. 25

Fig. 26A

Fig. 26B

0.00000 s
5.00 ms/div

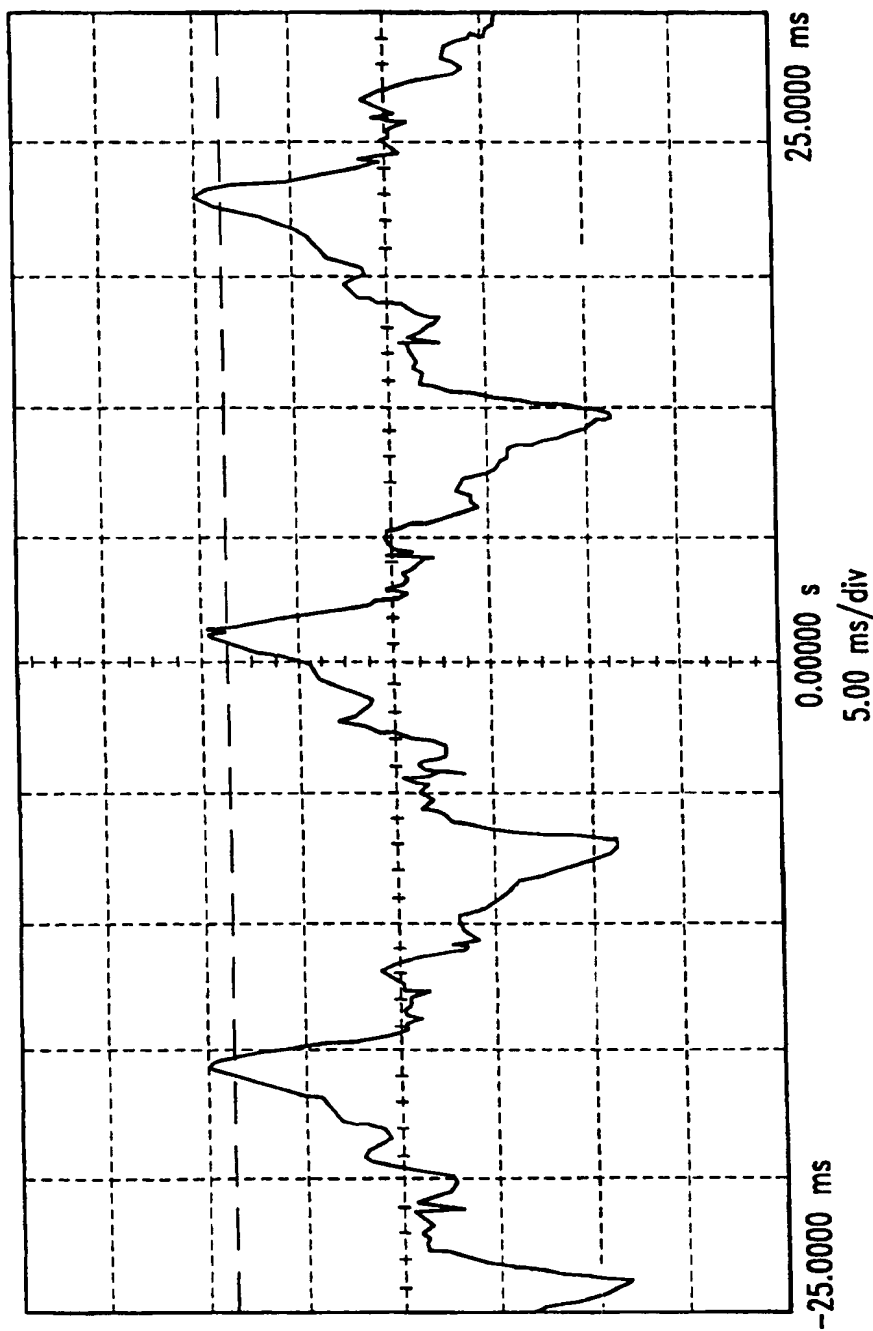


Fig. 26C

0.0000 s
5.00 ms/div
25.0000 ms

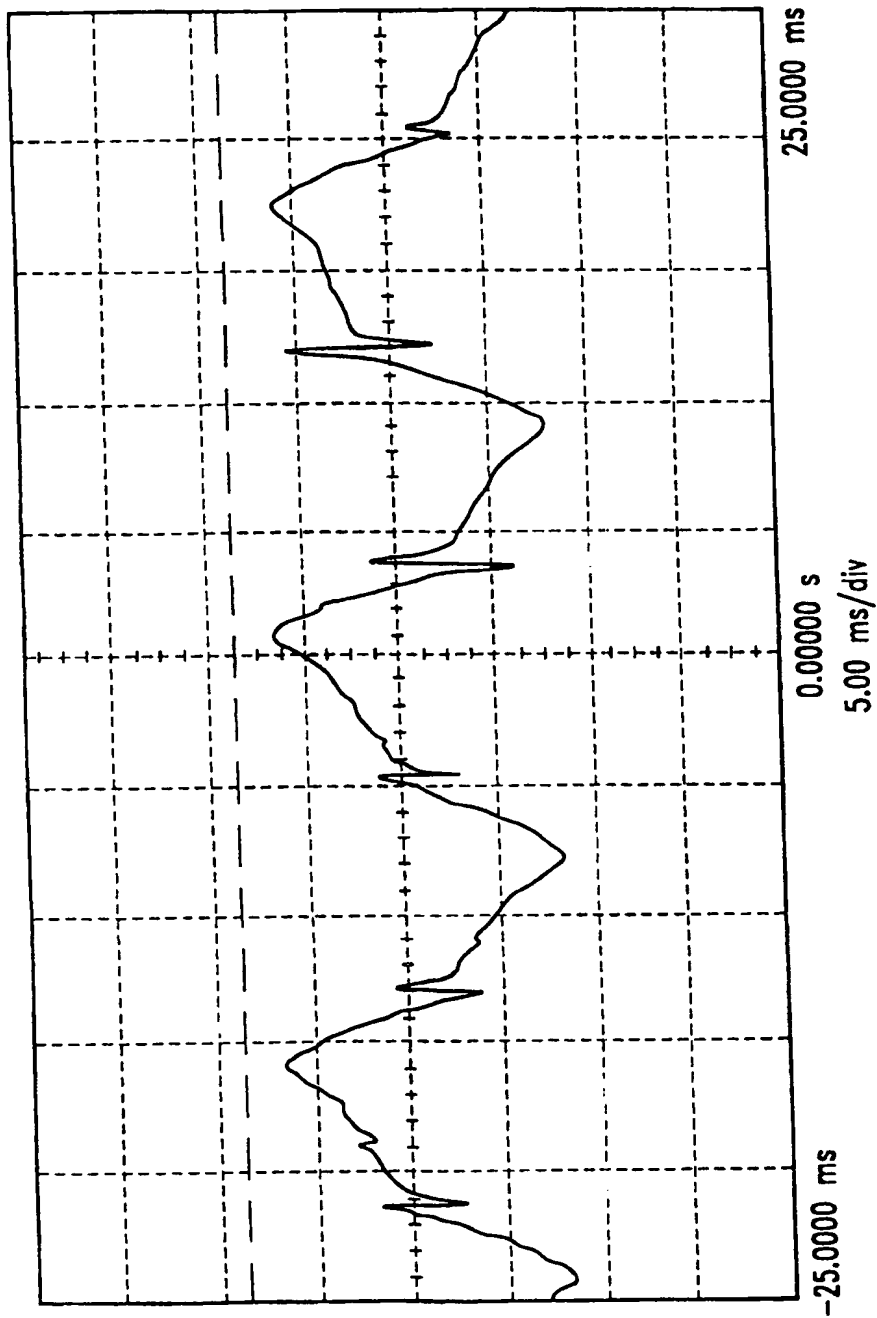


Fig. 26D

0.0000 s
5.00 ms/div
25.0000 ms

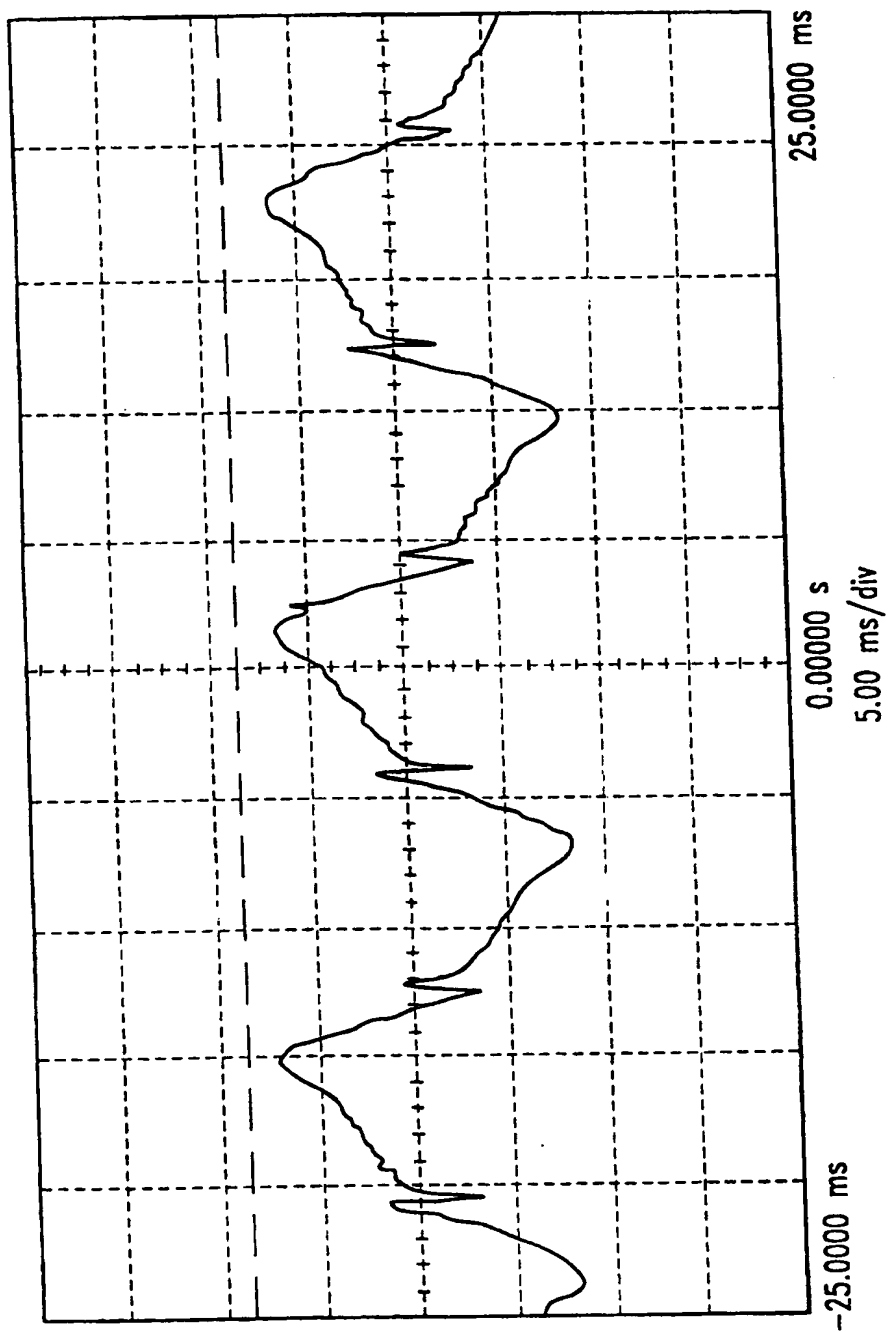


Fig. 26E

Fig. 27

[illegible]

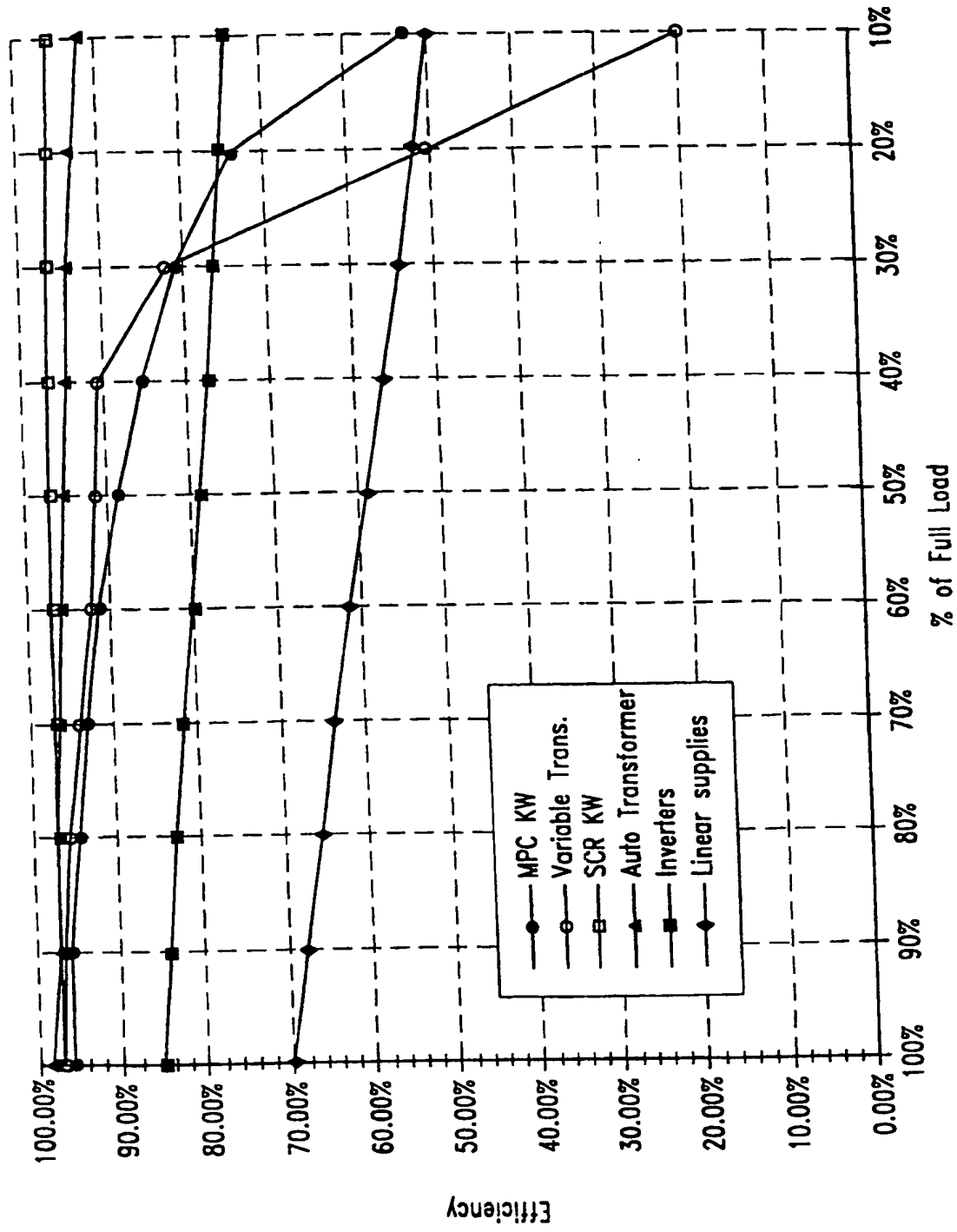


Fig. 28

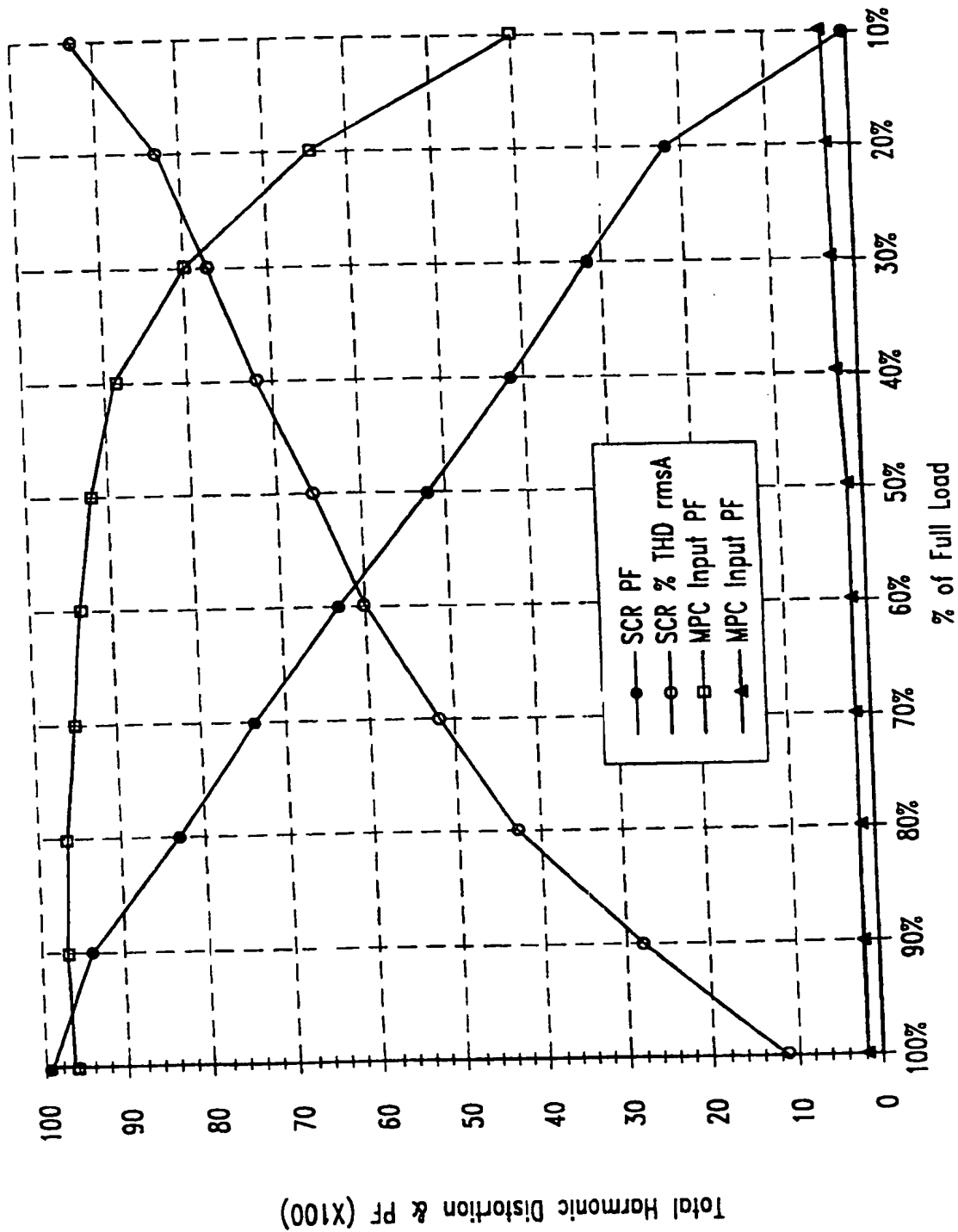


Fig. 29

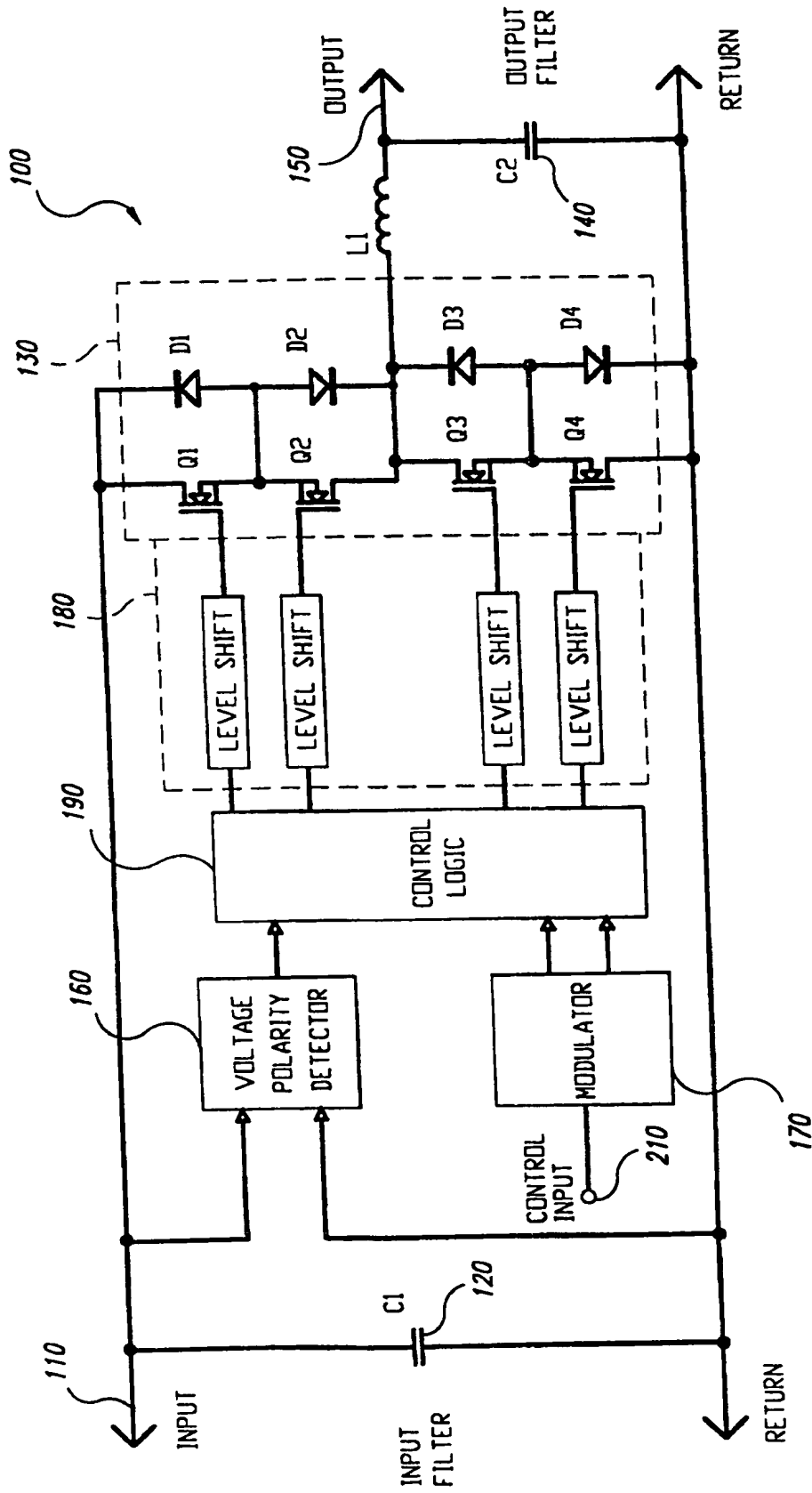


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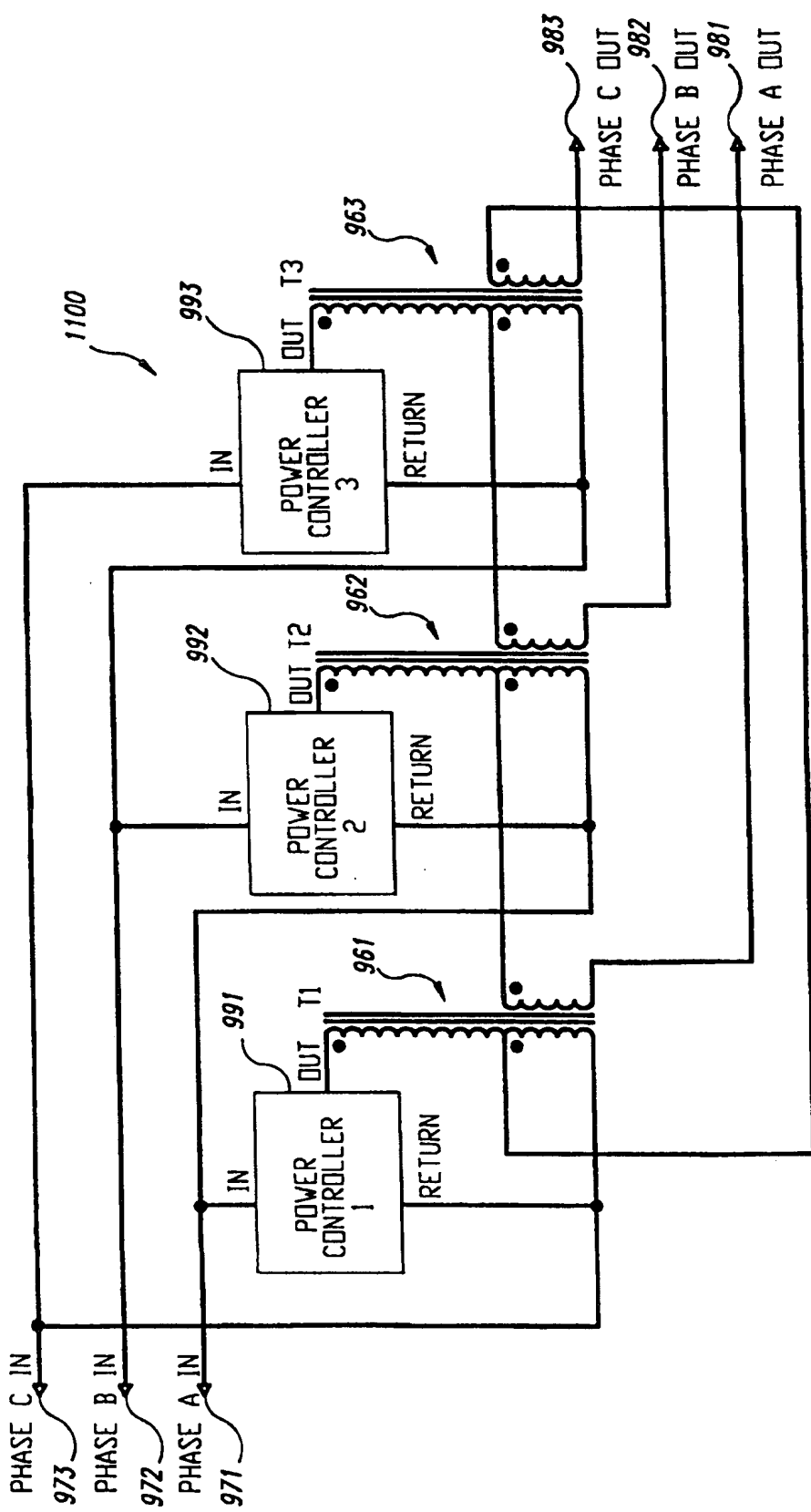


Fig. 31

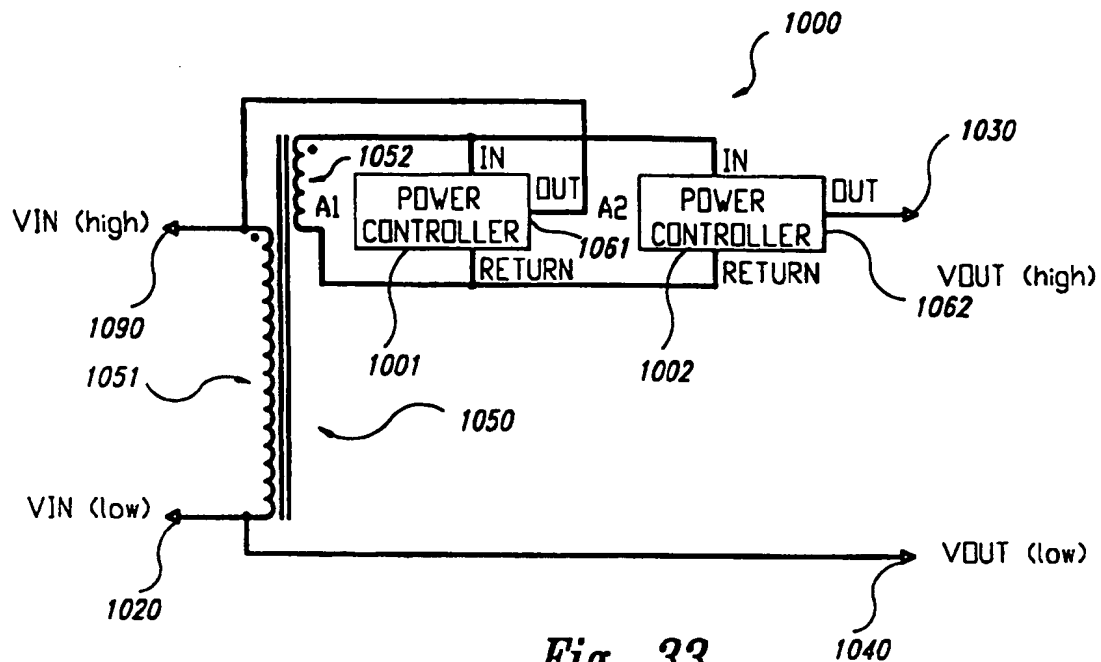


Fig. 33

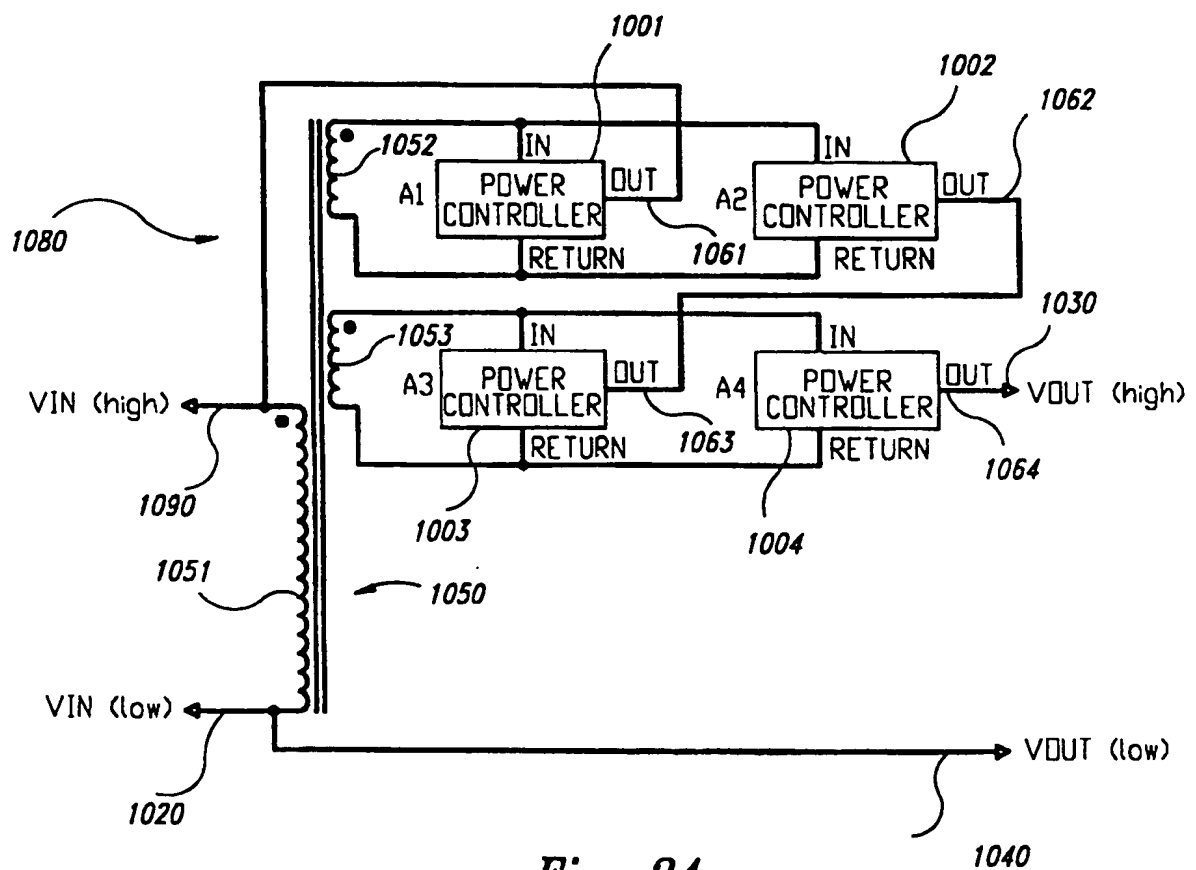


Fig. 34

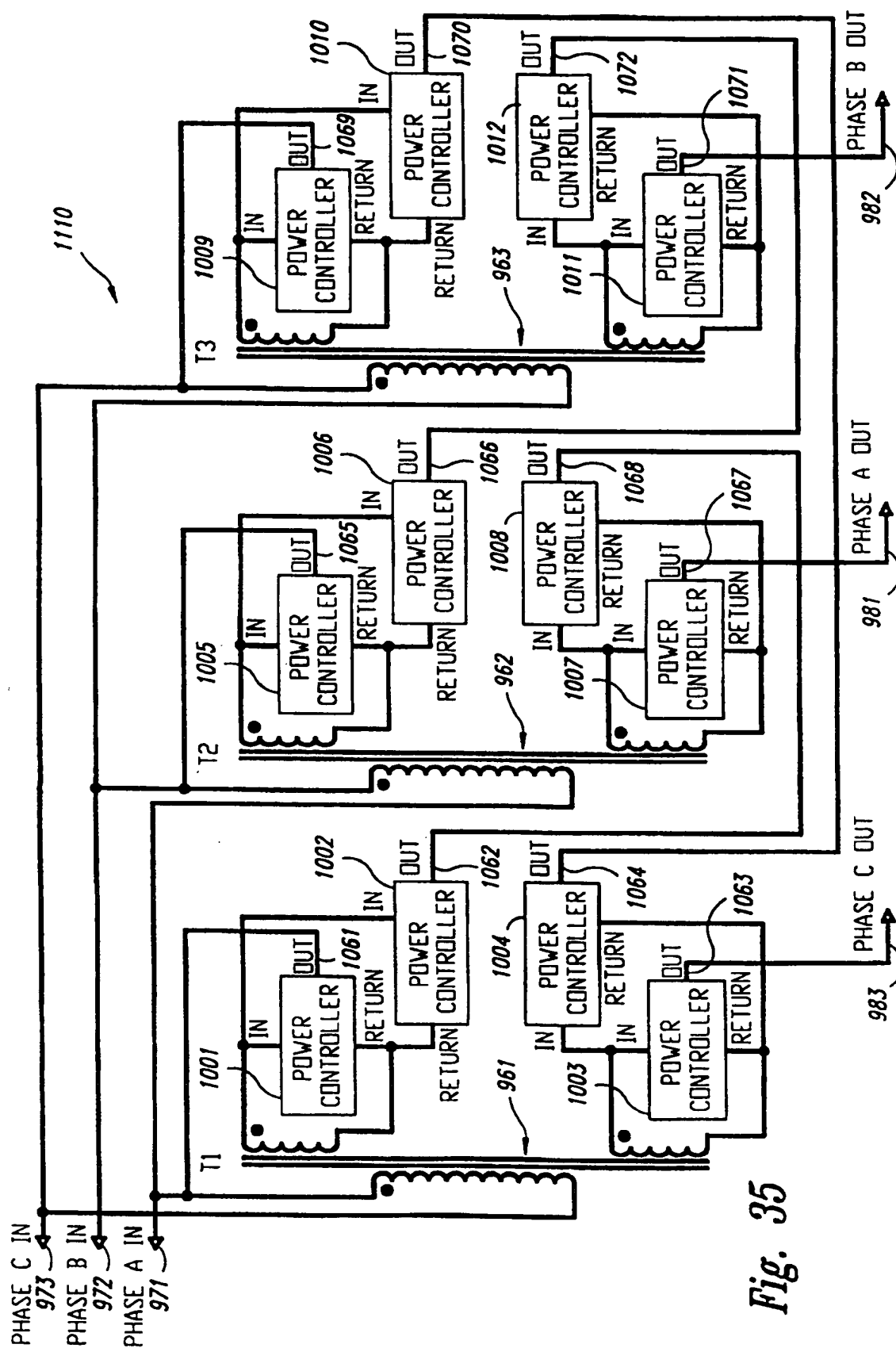


Fig. 35